Pioneer sound.vision.soul

Service Manual

ORDER NO. RRV2582

DVR - 7000

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Tyme	Model	Dower Poguirement	Dogion No	Domerko
Туре	DVR-7000	Power Requirement	Region No.	Remarks
WY	0	AC220-240V	2	
WV	0	AC220-240V	2	
WL	0	AC220-240V	3	

This service manual should be used together with the following manual(s):

Model	Order No.	Remarks		
DVR-7000/KU/CA	RRV2536	DVD Recorder		
DVR-A03	RRV2423	DVD-R/RW Drive Unit		

CONTENTS

1. SAFETY INFORMATION 2
2. CONTRAST OF MISCHELLANEOUS PARTS 4
3. BLOCKDIAGRAM AND SCHEMATIC DIAGRAM \cdots 14
4. PCB CONNECTION DIAGRAM ······ 42
5. ADJUSTMENT 50
6. GENERAL INFORMATION 53
6.1 MODEL TYPE AND REGION SETTING53
6.2 IC 54
7 PANEL FACILITIES AND SPECIFICATIONS 65

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1. SAFETY INFORMATION

This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.

Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING

This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to cause cancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 - Proposition 65

NOTICE

(FOR CANADIAN MODEL ONLY)

Fuse symbols – (fast operating fuse) and/or – (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE

(POUR MODÈLE CANADIEN SEULEMENT)

Les symboles de fusible — (fusible de type rapide) et/ou — (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

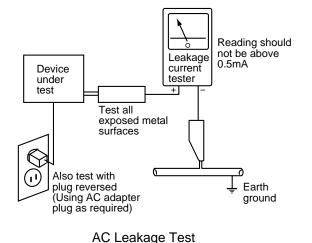
(FOR USA MODEL ONLY) -

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a Δ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

- IMPORTANT-

THIS PIONNER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

LASER DIODE CHARACTERISTICS MAXIMUM OUTPUT POWER: 35 mW WAVELENGTH: 658 nm

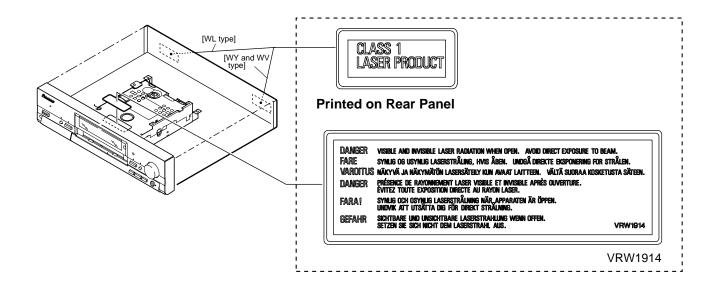
WARNING!

DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.



LASER
Picture 1
Warning sign for laser radiation

■ LABEL CHECK



Additional Laser Caution

- The ON/OFF(ON:low level,OFF:high level) status of the CLAMP signals for detecting the loading state are detected by the drive CPUs, and the design prevents laser diode oscillation when the CLAMP signal turns OFF.
 - In normal operation, if no disc is clamped, the laser diode oscillation is disabled.
 - However, the interlock does not always operate in the test mode. $\mbox{*}$
- When the cover is opened, close viewing of the objective lens with the naked eye will cause exposure to a Class 3A laser beam.

^{*} Refer to pages 43 of DVR-A03 Service Manual(RRV2423).

2. CONTRAST OF MISCELLANEOUS PARTS

NOTES: • Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.

- The $ilde{\Lambda}$ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- Screws adjacent to ▼ mark on product are used for disassembly.
- Reference Nos. indicate the pages and Nos. in the service manual for the base model.
- When ordering resistors, first convert resistance values into code form as shown in the following examples.
 Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).

 $5.62k \rightarrow 562 \times 10^{1} \rightarrow 5621 \dots RN1/4PC[5]6[2]1F$

CONTRAST TABLE

DVR-7000/WY, /WV, /WL and /KU/CA types are constructed the same except for the following:

Ref.		0 -1 -1 - 1 - 1 - 1 - 1 - 1		Part No.				
No.	Mark	Symbol and Description	DVR-7000 /KU/CA	DVR-7000 /WY	DVR-7000 /WV	DVR-7000 /WL	Remarks	
		PCB ASSEMBLIES						
		TUJB ASSY	VWM2103	VWM2104	VWM2104	VWM2112		
P7-1		⊢TUMJ ASSY	VWV1885	VWV1889	VWV1889	VWV1897		
P7-2		REAR JACK ASSY	VWV1887	VWV1891	VWV1891	VWV1883		
P7-3		-SECAM ASSY	Not used	VWV1892	VWV1892	VWV1892		
P7-3		-3D Y/C ASSY	VWV1888	Not used	Not used	Not used		
P7-4		FRONT JACK ASSY	VWV1886	VWV1890	VWV1890	VWV1890		
P7-5		MAIN ASSY	VWV1894	VWV1895	VWV1895	VWV1895		
		SCART ASSY	Not used	VWV1896	VWV1896	Not used	No.1	
P7-6	\triangle	POWER SUPPLY ASSY	VWR1347	VWR1348	VWR1348	VWR1348		
		PACKING SECTION						
P5-1		RF Antenna Cable	VDE1025	Not used	Not used	Not used		
P5-1		RF Antenna Cable (PAL)	Not used	VDE1075	VDE1075	VDE1075		
P5-4	\triangle	AC Power Cord	ADG7021	ADG1127	Not used	ADG1127		
	\triangle	AC Power Cord (T5A fuse inside)	Not used	Not used	ADG7004	ADG1156		
		SCART Cable	Not used	VDE1074	VDE1074	Not used		
P5-6	NSP	Warranty Card	ARY1026	ARY7022	ARY7022	Not used		
P5-7		Operating Instructions(English)	VRB1275	VRB1282	VRB1281	VRB1283		
		Operating Instructions(French)	Not used	VRE1089	Not used	Not used		
		Operating Instructions(German)	Not used	VRE1090	Not used	Not used		
		Operating Instructions(Italian)	Not used	VRE1091	Not used	Not used		
		Operating Instructions(Spanish)	Not used	VRE1092	Not used	Not used		
		Operating Instructions(Dutch)	Not used	VRE1093	Not used	Not used		
		Operating Instructions(Swedish)	Not used	VRE1094	Not used	Not used		
P5-8		Operating Instructions(Chinese)	Not used	Not used	Not used	VRE1097		
P5-9		Remote Control Unit	VXX2763	VXX2776	VXX2763	VXX2777		
P5-11	NSP	DVD-RW Disc Ver.1.1	VZZ1001	DVS-RW47B/E	DVS-RW47B/E	Not used		
P5-15		Packing Case	VHG2122	VHG2173	VHG2174	VHG2175		
		EXTERIOR SECTION						
P7-13		Housing Assy (10P)	VKP2264	VKP2276	VKP2276	VKP2276		
		Flexible Cable (21P)	Not used	VDA1877	VDA1877	Not used	No.2	
		Flexible Cable (25P)	Not used	VDA1878	VDA1878	Not used	No.3	
	NSP	PC Support	Not used	VEC1584	VEC1584	Not used	No.4	
		Spacer (for TUJB ASSY)	Not used	VEC2157	VEC2157	Not used	No.5	
P7-33		Rear Panel	VNA2328	VNA2330	VNA2334	VNA2408		
P7-37	NSP	Upper Plate Assy	VNE2272	Not used	Not used	Not used		
	NSP	Upper Plate	Not used	VNE2246	VNE2246	VNE2246	No.6	

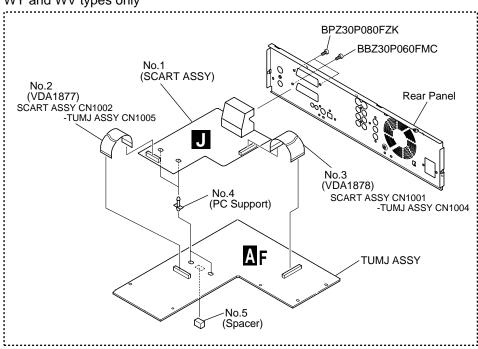
Ref.		Owner of the distriction		D			
No.	Mark	Symbol and Description	DVR-7000 /KU/CA	DVR-7000 /WY	DVR-7000 /WV	DVR-7000 /WL	Remarks
P7-62		Cooling Sheet S	VEB1333	Not used	Not used	Not used	
P7-69		65 Label	ARW7050	Not used	Not used	Not used	
P7-70		Fuse Caution Label	VRW1902	Not used	Not used	Not used	
P7-71		Fuse Caution Label	VRW1903	Not used	Not used	Not used	
		FRONT PANEL SECTION					
P9-7		Front Aluminium	VAH1392	VAH1378	VAH1378	VAH1378	
P9-17		Panel Base	VNK4983	VNK4799	VNK4799	VNK4799	
P9-18		Input Door	VNK4924	VNK4925	VNK4926	VNK4800	

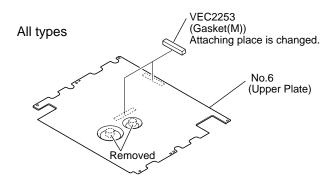
Notes: \bullet The numbers in the remarks column correspond to the numbers on "EXPLOEDED VIEWS".

• For ASSEMBLIES, refer to "CONTRAST OF PCB ASSEMBLIES", "PCB PARTS LIST" and "3. BLOCK DIAGRAM AND SCHE-MATIC DIAGRAM".

EXPLODED VIEWS

WY and WV types only





• CONTRAST OF PCB ASSEMBLIES

EF MAIN ASSY

VWV1895 and VWV1894 are constructed the same except for the following:

Morle	Sumbol and Description	Part	No.	Domonko
Mark	Symbol and Description	VWV1894	VWV1895	Remarks
	IC1008 (FLASH ROM)	VYW1922	VYW1927	
	IC4002 (SDRAM 16M)	Not used	MB81F161622C-80FN	*1
	IC7004 (SGRAM 16M)	M32L1632512A-8Q	Not used	
	IC7006 (Video Encoder)	PM0024AF	Not used	
	IC9502 (Stream Check)	UPD65954GC-E59-7EA		
	IC9503 (EPLD)	PDY078A	PDY076A	
	Q7001,Q7002	Not used	2SA1576A	*2
	Q7006,Q7008	2SA1576A	Not used	
	L3018	VTL1079	Not used	
	L7003,L7004,L7008-L7010	VTL1124	Not used	
	F0863	Not used	VTF1096	*3
	F8008	VTF1096	Not used	
	C1018	CEV221M4	VCH1234	
	C4012,C4014,C4027,C4029,C4035	Not used	CKSRYF104Z25	*1
		Not used		*2
	C7001,C7002	Not used	CKSRYF105Z10	**2
	C7095	CEV100M16	Not used	
	C7051	CEV101M16	Not used	
	C7003-C7005,C7058,C7065,C7101,C7104	CEV221M4	Not used	
	C7096,C7097,C9501-C9506,C9512-C9515	CKSRYF104Z25	Not used	
	C7006-C7009,C7044,C7059-C7064	CKSRYF105Z10	Not used	
	C7070,C7071,C7082,C7083,C7089,C7090	CKSRYF105Z10	Not used	
	C7099,C7102,C7103,C7108-C7111	CKSRYF105Z10 Not used		
	C7010,C7027,C7028,C7042,C7043,C7056	CKSQYF225Z16 Not used		
	C7100	CKSQYF475Z10	Not used	
	C0826	Not used	CCSRCH221J50	*3
	00444			
	C8111	CEV101M6R3	VCH1235	
	C8121,8126	CEV101M16	VCH1235	
	C8123,C8131	CCSRCH750J50	CCSRCH560J50	
	C8124,C8129	CCSRCH471J50	CCSRCH221J50	
	C8089,C8094,C8107,C8108,C8127	CKSRYF104Z25	CKSRYF105Z10	
	R3102	RS1/16S101J	Not used	
	R7072	RS1/16S470J	RS1/16S330J	
	R7025	RS1/16S103J	RS1/16S331J	
	R7001-R7003,R7007-R7009,R7016-R7018	Not used	RAB4C0R0J	
	R7100,R7129	Not used	RS1/16S0R0J	
	R7010-R7015	Not used	RS1/16S220J	*2
	R7205,R7206	Not used	RS1/16S101J	• •
	·			
	R7004,R7005	Not used	RS1/16S222J	'
	R7110 R7081,R7084,R7089,R7115,R7119	RS1/16S3300F RAB4C0R0J	Not used Not used	
	D7042 D7044 D7067 D7069	DAD4COOL	Not wood	
	R7042-R7044,R7067,R7068	RAB4C220J	Not used	
	R7006,R7019,R7037,R7041,R7046,R7047	RS1/16S0R0J	Not used	
	R7051-R7054,R7066,R7069,R7070,R7106	RS1/16S0R0J	Not used	
	R7107,R7114,R7116-R7118,R7121,R7122	RS1/16S0R0J	Not used	

Moule	Combal and Dagarintian	Part	No.	Remarks		
Mark	Symbol and Description	VWV1894 VWV1895				
	R7099	RS1/10S220J	Not used			
	R7036,R7045,R7095-R7098,R7101,R7130	RS1/16S220J	Not used			
	R7127,R7128	RS1/16S101J	Not used			
	R7090	RS1/16S332J	Not used			
	R7120	RS1/16S103J	Not used			
	R8074,R8116	RS1/16S5600F	RS1/16S8200F			
	R8018,R8020,R8021	RS1/16S0R0J	RS1/16S471J			
	R0808	0808 Not used RS1/10S0R0J		*3		
	R8063	RS1/10S0R0J	Not used			
	R8139,R8140,R8301,R8302	RS1/16S221J	Not used			
	R9503,R9506,R9515	Not used	RAB4C220J	*4		
	R9509-R9512,R9517,R9520,R9528	RAB4C220J	Not used			
	R9529,R9540,R9541	RAB4C220J	Not used			
	R9508,R9576	RS1/16S0R0J	Not used			
	R9538,R9539,R9701,R9702	RS1/16S220J	Not used			
	R9516	RS1/16S103J	Not used			
	VR7001,VR7002 (100Ω)	Not used	VCP1167	*2		
	VR7006,VR7007 (470Ω)	VCP1169	Not used			

^{*1} Refer to " 3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM" page 32.
*2 Refer to " 3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM" page 35.
*3 Refer to " 3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM" page 36.
*4 Refer to " 3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM" page 38.

F POWER SUPPLY ASSY

VWR1348 and VWR1347 are constructed the same except for the following:

Mark	Symbol and Description	Part	No.	Remarks		
IVIAIK	Symbol and Description	VWR1347	VWR1348	Remarks		
	Q110	VZF1108	VZF1096			
		(2SK2750)	(2SK2700)			
	Q120	VZF1101	VZF1095			
		(2SK2543)	(2SK2717)			
	Q412	VZF1113	VZF1122			
		(2SA954L)	(2SA1315)			
	D110	VZF1105	VZF1123			
		(HZS2C3)	(HZS3B3)			
	D103	UK1V26	Not used			
\triangle	FU101	VEK1044	AEK1059			
		(3.15A)	(T3.15A)			

Notes: • The upper contrast table is restricted to the service parts.

A F TUMJ ASSY

VWV1889 and VWV1897 are constructed the same except for the following:

Maule	Combal and Daggintian	Part	No.	Domonico
Mark	Symbol and Description	VWV1889	VWV1887	Remarks
	IC1371	UPC4570G2	Not used	
	IC1951	PST9146N	Not used	
	Q1951	DTA124EUA	Not used	
	Q1952	HN1C01FU	Not used	
	Q1953	2SA1576A	Not used	
	D1951-D1954,D2186	MA111	Not used	
	D1955	EP10QY03	Not used	
	C1371	CEAT101M16	Not used	
	C1954	CEAT471M6R3	Not used	
	C1372,C1951,C1952	CKSRYF104Z25	Not used	
	R1010,R1014,R1021	Not used	RS1/16S75R0F	
	R1040,R1046,R1047,R1063,R1064	Not used	RS1/16S0R0J	
	R2165,R2186	Not used	RS1/16S103J	
	R1048,R1050,R1062,R1065,R1066	RS1/16S0R0J	Not used	
	R1371,R1372,R1374–R1377	RS1/16S0R0J	Not used	
	R1958,R2112	RS1/16S220J	Not used	
	R1960	RS1/16S102J	Not used	
	R1954,R1957,R1965,R1966,R2030	RS1/16S103J	Not used	
	R1952,R1955,R1956	RS1/16S223J	Not used	
	R1953	RS1/16S473J	Not used	
	R1951	RS1/16S683J	Not used	
	R1959	RS1/16S104J	Not used	
	CN1004 (25P FFC Connector)	VKN1429	Not used	
	CN1005 (21P FFC Connector)	VKN1425	Not used	

BF REAR JACK ASSY

VWV1891 and VWV1883 are constructed the same except for the following:

Mark	Combal and Dagarintian	Part	No.	Domonto
Wark	Symbol and Description	Symbol and Description VWV1891 VW		Remarks
	Q1501,Q1503	Not used	2SD2114K	
	C1507,C1508	CCSRCH471J50	Not used	
	R1531,R1532,R1535	Not used	RS1/16S75R0F	
	R1518,R1523,R1528,R1533,R1534	Not used	RS1/16S0R0J	
	R1536,R1538,R1541,R1547,R1548,	Not used	RS1/16S0R0J	
	R1550,R1551	Not used	RS1/16S0R0J	
	R1537,R1540	Not used	RS1/16S101J	
	R1539,R1543–R1545	Not used	RS1/16S471J	
	R1581–R1586	RS1/16S0R0J	Not used	
	JA1522	Not used	VKB1522	

• PCB PARTS LIST

Mark		Description	Part No.	Mark	No.	Description	Pa	rt No.
Λ	T1184	L A C C V / / / / / / / / / / / / / / / / /			Q2014			RN2903
Аг	I UIVI	J ASSY(VWV1889)				, D1955, D1956		EP10QY03
SEMI	COND	JCTORS				D1103 D1401	,D1951–D1954	EP10QY03 MA111
Δ	IC2002		BA033FP			–D2023, D2041		MA111
	IC2013		BA10393F			,	,	
	IC4402 IC1102		BA4558F–HT BA7046F			,D4302, D4501		MA111
	IC1102		BA7665FS	A	D4101			UDZ33B
	101001		27.17 0001. 0	Δ		, D4602 –D4727		UDZS6.8B UDZS6.8B
		, IC5501	BR24E16FV	\triangle	D4723			UDZS8.2B
	IC4201		BU4052BCFV	_				
	IC7001 IC1002		LC74793JM MM1114XF	COIL	S AND	FILTERS		
		, IC1004, IC1171	MM1118XF			, L1412		LCTA100J2520
		, , -	-			, L7031		LCTA470J2520
	IC4702		MSP3417G		L4161			LCYA150J2520
	IC2003		PE5322C9		L4162			LCYA220J2520
Δ	IC2011 IC2017		PQ12RF11 PST9120N		L4163			LCYA330J2520
	IC2017		PST9130N		L4164			LCYA3R3J2520
					F1202	, F1204, F1206,	F3241, F3242	VTF1166
	IC1951		PST9146N		F1821	, F2007–F2009,	F4701-F4703	
	IC2008		RV5C386A			, F7002		VTF1170
	IC1421	, IC2001, IC2012, IC7003	SN74AHC1G08HDCK SN74AHC2G126HDCT		L4152,	, L4153		VTL1075
	IC2004		SN74AHC2GU04HDCT		L4101	, L4102, L7003		VTL1096
	IC1001	, IC1103	SN74LV4052APW					
		, IC3222	TC4W53FU	CAP	ACITOF			
	IC1101		TC74HC123AF			, C2043	00000	CCSRCH100D5
		i, IC2301	TC74VHCT541AFT			, C1337, C2029 , C4151	, C2030	CCSRCH101J50
	IC4701	, IC7002	TC7SET08FU				. C1115. C4325	CCSRCH101350
	IC4101	, IC7006	TK15404M		C4334		, 0 , 0	CCSRCH102J50
		, IC1902, IC3241	TK15420M					
	IC1312	!	TK15453V				, C4216, C4303	CCSRCH220J50
		, IC4202, IC4302	UPC4570G2		C4333	, C2202, C2203	C4164	CCSRCH220J50 CCSRCH221J50
	Q1103	, Q1106, Q1203, Q1207	2SA1576A		C4502		, 04104	CCSRCH470J50
	Q1211		2SA1576A		C4162	, C4718, C4719		CCSRCH560J50
		, Q3211, Q4308	2SA1576A					
\triangle	Q2006	, Q4411, Q4413	2SB1132			, C7031		CCSRCH680J50
	Q2002		2SB1237X		C4721	, C4722		CCSRCJ3R0C50 CEANP2R2M50
	Q1311	, Q1411, Q2023, Q2203	2SC4081			, C4108, C4111	, C4118	CEAT100M50
	Q3221	, Q3222, Q4102, Q4108	2SC4081				-C4223, C4320	
		, Q4162	2SC4081					
\triangle		, Q2004	2SD1664			, C4705, C4712		CEAT100M50
	Q2007		2SD1664			, C1014, C1024 C1118 C1175	, C1112 , C1201, C1204	CEAT101M10 CEAT101M10
Δ	Q3431	, Q4301	2SD1664				, C1401, C1402	
	Q4401	, Q4406	2SD1664			, C1831, C1834		CEAT101M10
		, Q2010, Q2022, Q4345	2SD2114K		00045	00000 00000	00005 0005	OF A T4 C 4 L 4 C
	Q4355		2SD2114K			-C2020, C2022 . C2041. C2049	, C2025, C2032	
	Q1104		2SK210				, C2054 , C2062, C2072	CEAT101M10 CEAT101M10
	Q1108	, Q1951, Q2001, Q2021	DTA124EUA		C2302	, C3431, C3434	, C4103, C4106	CEAT101M10
	Q1172	, Q1341, Q2013, Q2024	DTC124EUA				, C4348, C4410	
	Q3223	,Q7002	DTC124EUA		O 4 · · · =	04444 04415	04400 0:=5:	OF A T 10 11 11 1
	Q2003	, Q2005, Q4412, Q4414	DTC143EUA				, C4432, C4701 , C7001, C7011	
		, Q1113, Q1223, Q1224	HN1A01FU				, C7001, C7011 , C1106, C1371	
	Q1227	, Q1228, Q1231, Q1232	HN1A01FU		C1804	, C1811, C1812	, C1901, C1903	CEAT101M16
	Q3212	,Q4304,Q4305	HN1A01FU				, C3227, C3235	
		, Q4104	HN1B01FU		005:	0.406.4 6 :=:	0.400= .5 :=	0547/2/
	Q1114	, Q1115, Q1952, Q2202	HN1C01FU				, C4307, C4310	
		, Q2012, Q2015, Q2016	HN1K03FU			, C4431, C4433 , C2027		CEAT101M16 CEAT101M25
	Q4107	,Q4601, Q7001	HN1K03FU		C1320	•		CEAT101M25
	Q4201		RN1903			, C1009, C1012	, C1013	CEAT1R0M50
	~ ·= · ·							

Mark	No.	Descri	ption		Pa	rt No.	Mark	No.	Description	Part No.
							OTHE	RS		
	C1032,	C1033,	C1171,	C7005,	C7006	CEAT1R0M50	OIIIL		TV Turner Deals	V/VE4007
	C1356,	C1358				CEAT220M25		TU4101		VXF1007
	C1414					CEAT221M6R3		CN2003		12PL-FJ
	C4706					CEAT3R3M50		CN3001		B10B-ZR
	C1054,	C1057,	C1415			CEAT470M16		CN2001		B16B-PH-K
								JA1401	Optical Link Out	GP1FA551TZ
	C2067					CEAT471M16		011000		=
	C1058,	C1322,	C1324,	C1355,	C1357	CEAT471M6R3		CN2009		HLEM20S-1
		C1954,		,		CEAT471M6R3			, CN2007 Plug 2P	KM200SA2
	C7007	,				CEAT4R7M50			JA4502 Jack	RKN1004
	C2039					CEHAZA221M6R3		JA1411	Jack	VKB1074
								CN2008	7P Connector	VKN1267
	C1127,	C4105.	C4107,	C4114,	C4121	CKSRYB102K50				
	C4344,		,	,		CKSRYB102K50			, CN1002 B to B Connecto	
			C1023.	C1176.	C1412	CKSRYB103K50			20P Connector	VKN1424
						CKSRYB103K50			21P Connector	VKN1425
		C4169,				CKSRYB103K50			22P Connector	VKN1426
	• ,	C ,	0.0.0,	0.000		5.15.112.155.155		CN1004	25P Connector	VKN1429
	C1004.	C1011.	C1034.	C1105.	C1318	CKSRYB104K16				
		C1359,				CKSRYB104K16		CN3002	Connector	VKN1626
	C1319,		,	0		CKSRYB105K6R3		1001	Screw Plate	VNE1948
	C4318,					CKSRYB472K50			, KN3203, KN3204	VNF1084
	C4347,					CKSRYB473K25		X2002	(32.768kHz)	VSS1143
	04347,	04337				CRORT B47 SR25		X2001	(6.25MHz)	VSS1162
	C7008					CKSRYB563K16				
		C1009	C1015	C1025	C1102	CKSRYF104Z25		X7001	(17.734MHz)	VSS1177
						CKSRYF104Z25			(18.432MHz)	VSS1178
						CKSRYF104Z25			,	
							Б.			
	C11//,	C1203,	C1206,	C1209,	C1224	CKSRYF104Z25	БF	REAR	JACK ASSY	
	C1226	C1220	C1222	C1226	C1220	CKSBVE104725				
						CKSRYF104Z25	SEIVII	CONDU	CIURS	
						CKSRYF104Z25		Q1502		2SA1576A
					C2005	CKSRYF104Z25		Q1504,	Q1505	2SD2114K
		C2010,			00004	CKSRYF104Z25	CAPA	CITOR	S	
	C2023,	C2024,	C2026,	C2028,	C2031	CKSRYF104Z25	OAI 7			0000011474 150
	00000	00004	00000	00000	00040	01/00/15404705		C1507,	C1508	CCSRCH471J50
						CKSRYF104Z25				
					C2053	CKSRYF104Z25	RESIS	STORS		
		C2061,				CKSRYF104Z25			R1503, R1505, R1519	RS1/16S75R0F
						CKSRYF104Z25		R1520,F		RS1/16S75R0F
	C2201,	C2301,	C3212-	-C3214,	C3222	CKSRYF104Z25		Other R		RS1/16S□□□J
						01/05\/5/6/55		Otherix	63131013	K31/1035
						CKSRYF104Z25				
						CKSRYF104Z25	OTHE	:RS		
						CKSRYF104Z25		JA1501	3P Pin Jack	VKB1115
						CKSRYF104Z25		JA1521	Jack	VKB1173
	C4411,	C4413,	C4415,	C4425,	C4426	CKSRYF104Z25		CN1501	, CN1502 B to B Connector	VKN1392
								1501	Screw Plate	VNE2247
		C4430,				CKSRYF104Z25				
	C4707,	C4708,	C4716,	C4717,	C5502	CKSRYF104Z25	\mathbf{C}			
		C7012,				CKSRYF104Z25	G F	SECA	M ASSY	
	C1114,	C1316,	C1321,	C1328,	C1353	CKSRYF105Z10	<u> </u>		OTODO.	
	C1360,	C1413,	C1833,	C2059,	C2077	CKSRYF105Z10	SEMI	CONDU	CIORS	
								IC3601		MM1394AF
	C3433,	C7016				CKSRYF105Z10		IC3651		SN74AHC2G14HDCT
	C2042,	C2045				PCH1132		IC3501		TB1274AF
	•							IC3512		TC7SH32F
DECI	STORS							IC3511		TC7WH123FU
KESI		_	_	_						
		R1330,			_	RS1/10S0R0J		IC3621		TC7WU04FU
			R3241,	R4169,	R4410	RS1/10S0R0J		IC3551		TK15420M
	R3245,					RS1/16S1801F		Q3531.	Q3541, Q3551, Q3573	2SA1576A
	R1348,	R3244,	R3251			RS1/16S2201F		Q3574		2SA1576A
	R1347					RS1/16S3901F		Q3571,	Q3572	2SC4081
								,		
						RS1/16S4700F		Q3501		RN1903
						RS1/16S4700F		D3651		EP10QY03
						RS1/16S5601F				
				R1041-	-R1043	RS1/16S75R0F	COIL	C AND F	III TEDO	
	VR414	1 (2.2KΩ	2)			ACP1090	COIL		FILTERS	
								L3531, I	_3541	LCKA151J2520
		1-VR190		(Ω)		ACP1091		L3551		LCTA560J2520
	Other F	Resistors				RS1/16S□□□J		L3552		LCTA680J2520

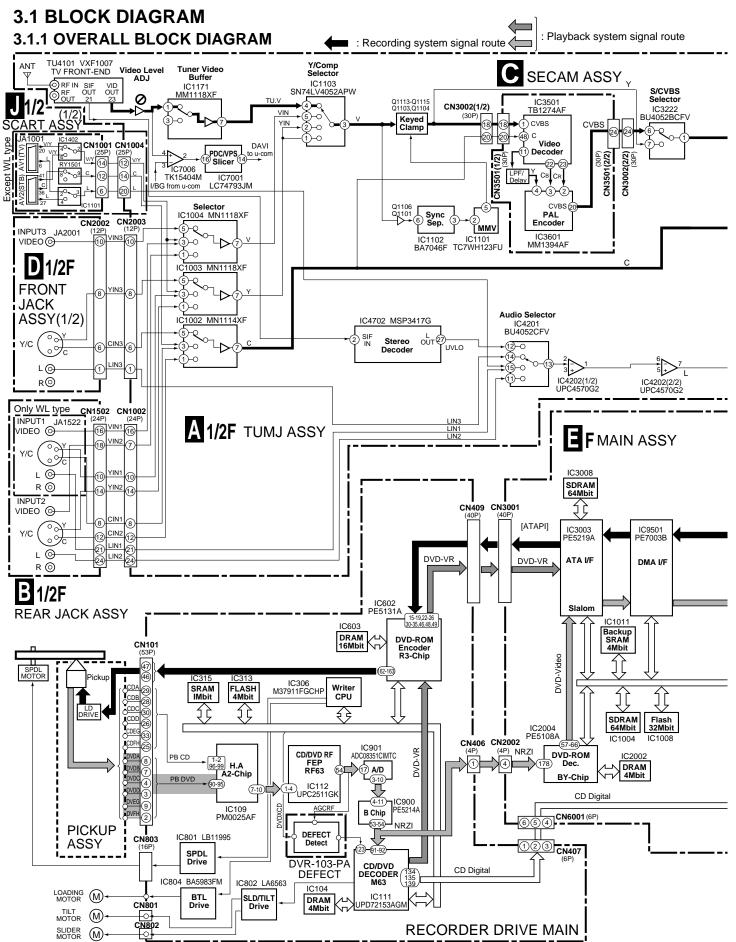
Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	F3551		VTF1176				
C A D A	CITOE	10		J	SCAF	RT ASSY	
SAPA	COSTAN		CCSRCH102J50	SEM	ICOND	UCTORS	
	C3553	-C3520	CCSRCH102J50 CCSRCH120J50		IC100		BA4558F-HT
	C3555		CCSRCH150J50			1, IC1352	BU4066BCF
		, C3621, C3622	CCSRCH220J50		IC150	ı 4, IC1405	MM1113XF MM1228XF
	C3533	, C3543	CCSRCH221J50		IC140		MM1231XF
	C3531	, C3541	CCSRCH470J50		10440		MM4500VAI
	C3653		CCSRCH471J50		IC1402	2 6, IC1507	MM1503XN MM1506XN
		, C3557	CCSRCH680J50			2, IC1503, IC1505	MM1509XN
	C3503 C3532	, C3542	CCSRCH7R0D50 CCSRCH9R0D50		IC140°	1	MM1511XN
					IC1403	3	SN74AHC2G53HD
		, C3607	CEANP1R0M50		IC130	1	SN74LV595APW
		, C3611 , C3601, C3604, C3652	CEAT100M50 CEAT101M10		IC1504	1	TC7SET32FU
	C3551	, C3571	CEAT101M16			1, IC1202, IC1203	TK15324M
	C3508		CEAT2R2M50	٨	Q1053	2–IC1105, IC1201	UPC4570G2
	C2512	C2545	CE AT470M46	Δ	Q1053	1	2SA1576A
	C3506	, C3515	CEAT470M16 CEAT4R7M50			, Q1207, Q1210, Q1306	2SA1576A
	C3505		CEATR47M50	Δ	Q1052	, Q1355	2SB1132 2SC4081
		, C3509, C3623	CKSRYB103K50		Q1204 Q1054		2SD1664
	C3510	, C3511	CKSRYB104K16			, Q1203, Q1205, Q1206	2SD2114K
		, C3517	CKSRYB105K6R3		O1212	–Q1215, Q1305	2SD2114K
	C3507		CKSRYB223K50			, Q1353, Q1501	DTA124EUA
	C3501	, C3513, C3514, C3521, C35 , C3572, C3573, C3602, C36	22 CKSRYF104Z25		Q1358		DTA143EUA
		, C3651	CKSRYF104Z25			, Q1055, Q1208, Q1209	DTC124EUA
					Q1303	, Q1304, Q1351, Q1354	DTC124EUA
RESI	STORS					,Q1360, Q1361, Q1502	DTC124EUA
		, R3625	RS1/10S0R0J			, Q1359	DTC143EUA
	R3531 R3543	, R3541, R3576, R3579	RS1/16S1001F RS1/16S1002F	Δ	D1351	–D1361, D1501	1SS355 UDZ12B
	R3532		RS1/16S1801F	44		-D1304	UDZS6.2B
	R3604		RS1/16S1802F			B	
	R3606		RS1/16S3902F		D1601	–D1612, D1701–D1712	UDZS9.1B
		, R3578	RS1/16S4700F	COII	SAND	FILTERS	
	R3533		RS1/16S8201F	00.2		-L1623, L1625, L1713-L1	717 VTL1086
	Other I	Resistors	RS1/16S□□□J			, L1721, L1723	VTL1086
THE	ERS			CVA/IT	-01150	AND DELAYO	
	CN350	1 Plug	VKN1797	SWII		AND RELAYS	VCD4040
	3001	Screw Plate	VNE2247		KY135	51, RY1501	VSR1016
		(16.20MHz) (4.433619MHz)	VSS1175 VSS1176	CAP	ACITOR	RS	
		,				, C1105, C1108, C1112, (C1113 CCSRCH220J50
DF	FROI	NT JACK ASSY				, C1119, C1120, C1219, (
		JCTORS				-C1606, C1701-C1706 , C1109, C1114, C1118	CCSRCH471J50 CEAT100M50
			UD700 4D			, C1109, C1114, C1116	CEAT100M50
	D2010-	-D2013	UDZS9.1B				
RESI	STORS					-C1218, C1358, C1406-0 , C1420, C1425, C1502, 0	
		Resistors	RS1/16S□□□J			, C1420, C1423, C1502, C , C1523, C1524, C1527, (
	2 01 1				C1052	, C1353, C1402, C1403, G	C1415 CEAT101M10
THE	ERS				C1417	, C1429, C1501, C1504, C	C1512 CEAT101M10
	CN200	2 Jack	12R-FJ		C1515	, C1521, C1522	CEAT101M10
	CN200		B6B-PH-K			, C1005, C1055, C1101, (
	JA2001		VKB1169		C1208		CEAT101M16
	JA2002		VKB1170 VKB1171		C1054		CEAT101M25
	JA2003	DA LEIIIIIIIIIII	וווטאא		C1412	, C1423, C1525, C1529	CEAT102M6R3
	KN200	1, KN2002 Earth Metal Fittin	g VNF1084		C1410	, C1411, C1413, C1421, (C1422 CEAT1R0M50
					C1427		CEAT1R0M50
					C1510		CEAT220M25
					C1509		CEAT471M6R3

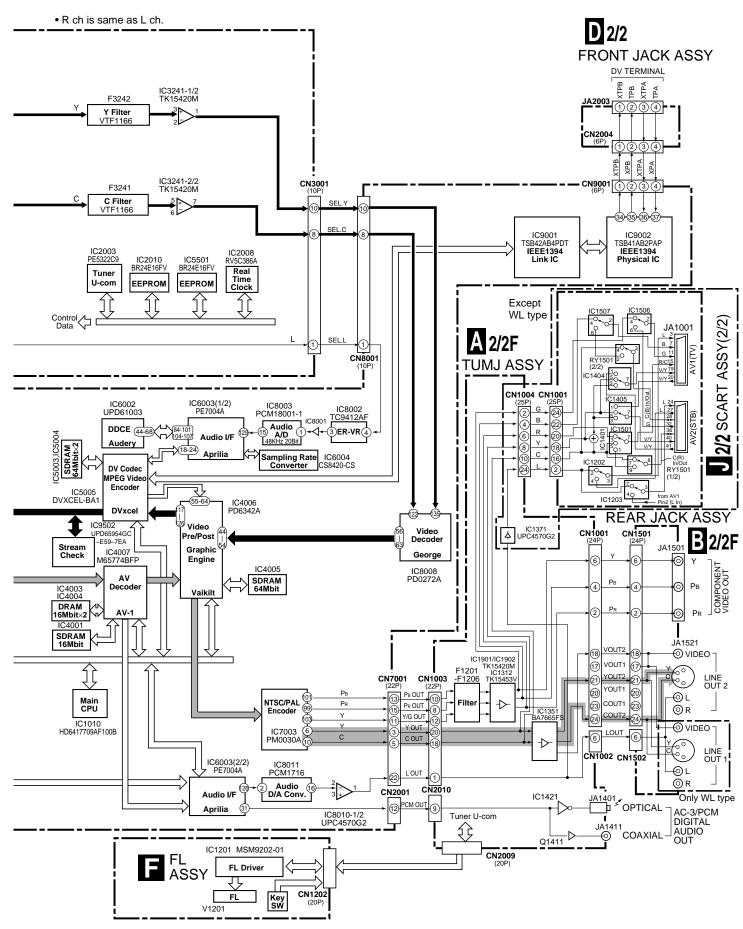
DVR-7000

Mark	No.	Description	Pa	art No.
	C1424,		,	CKSRYB102K50 CKSRYB103K50 CKSRYB104K16 CKSRYB104K16 CKSRYB104K16
	C1111,			CKSRYB104K16 CKSRYF104Z16 CKSRYF104Z25 CKSRYF104Z25 CKSRYF104Z25
	C1416,			CKSRYF105Z10 CKSRYF105Z10 CKSRYF105Z10
RESIS	R1609, R1709,	R1503, R1506	, R1507, R1510 , R1615, R1617	
OTHE	AND THE PROPERTY OF THE PROPER	2 21P Conec	ctor	VKB1161 VKN1425 VKN1429 VNE1948

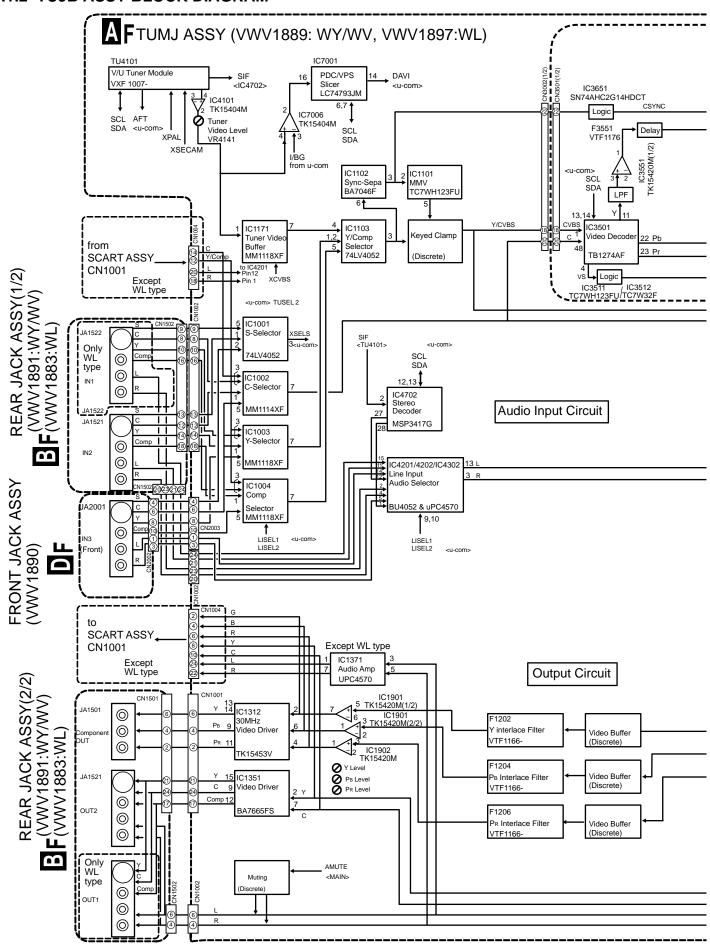
DVR-7000

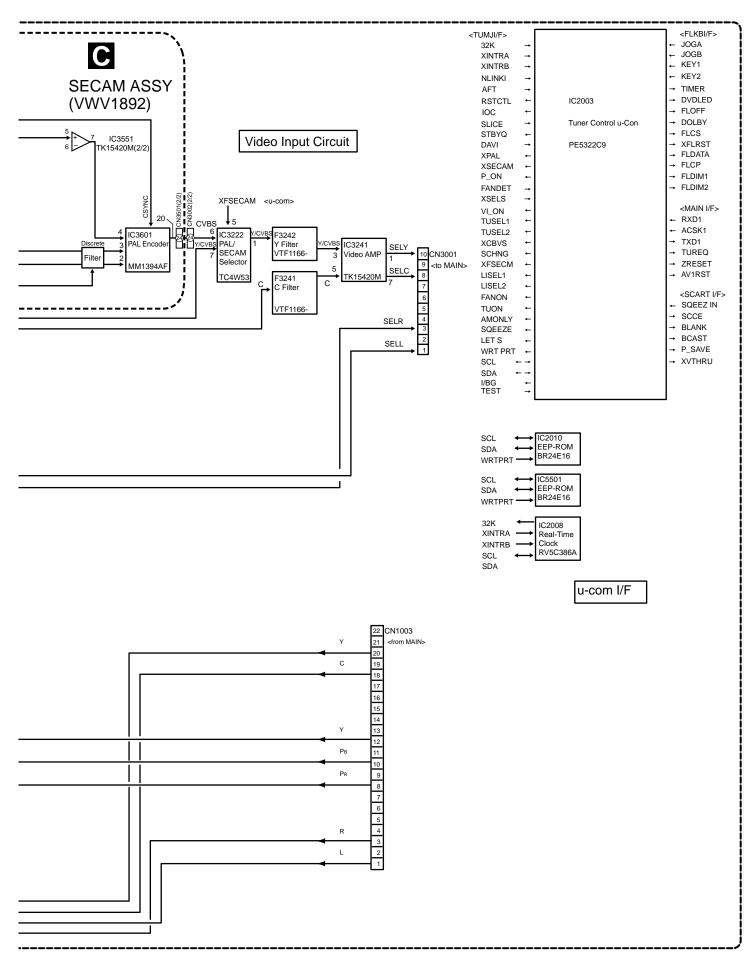
3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM



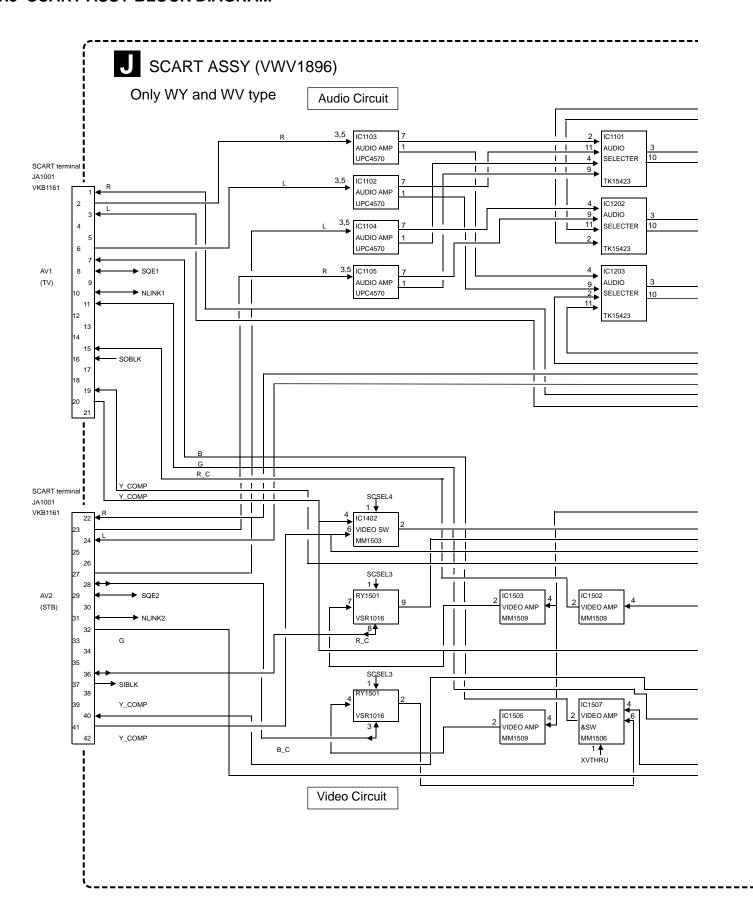


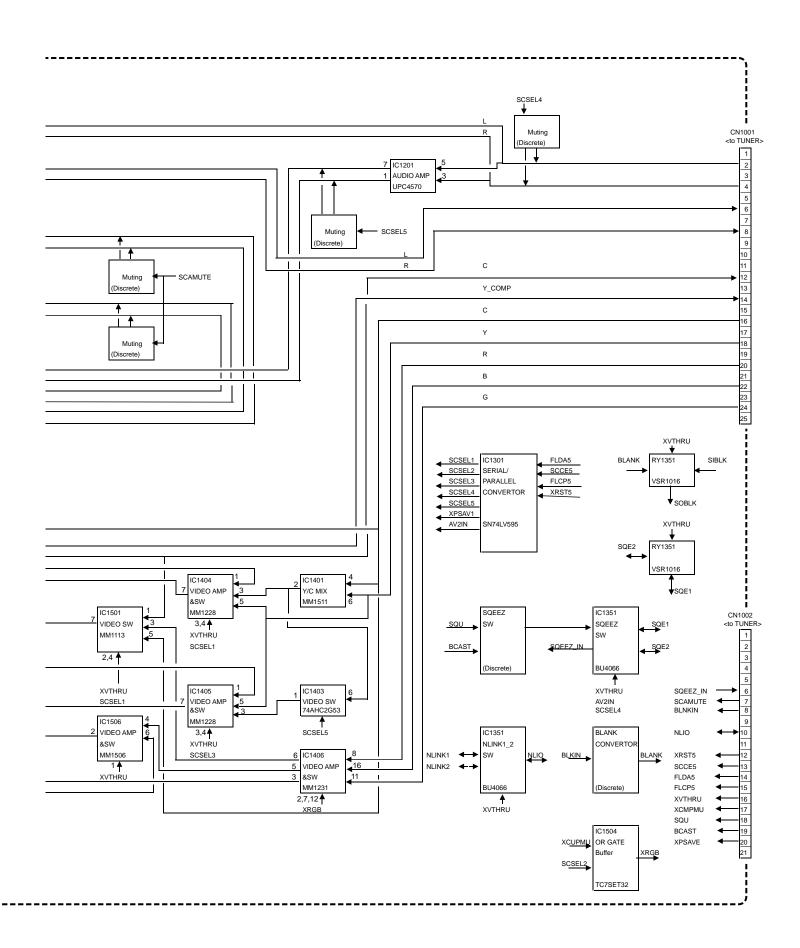
3.1.2 TUJB ASSY BLOCK DIAGRAM



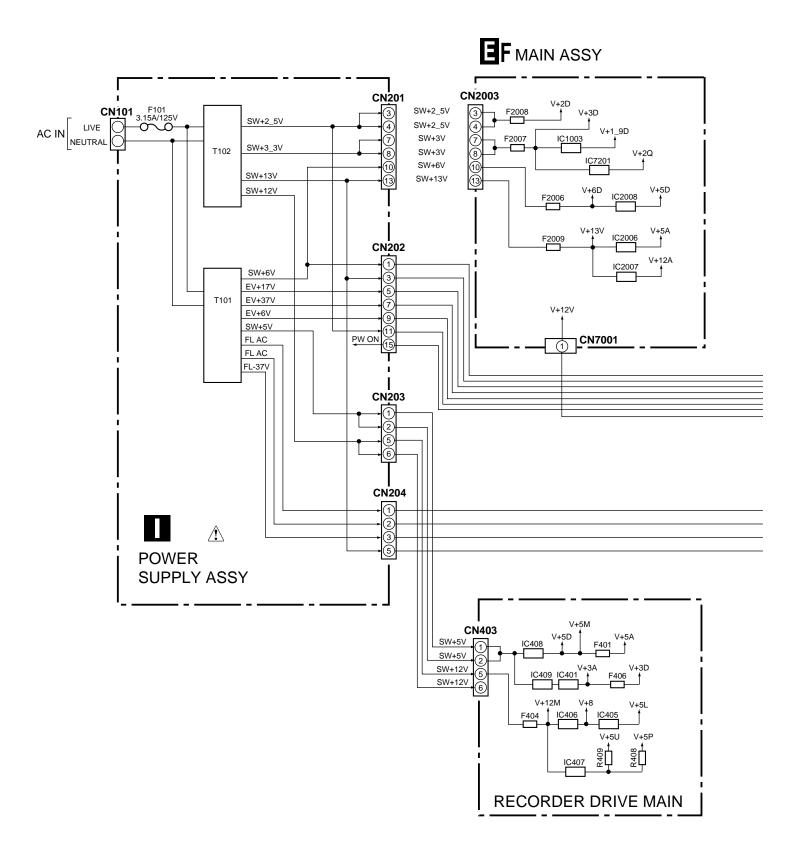


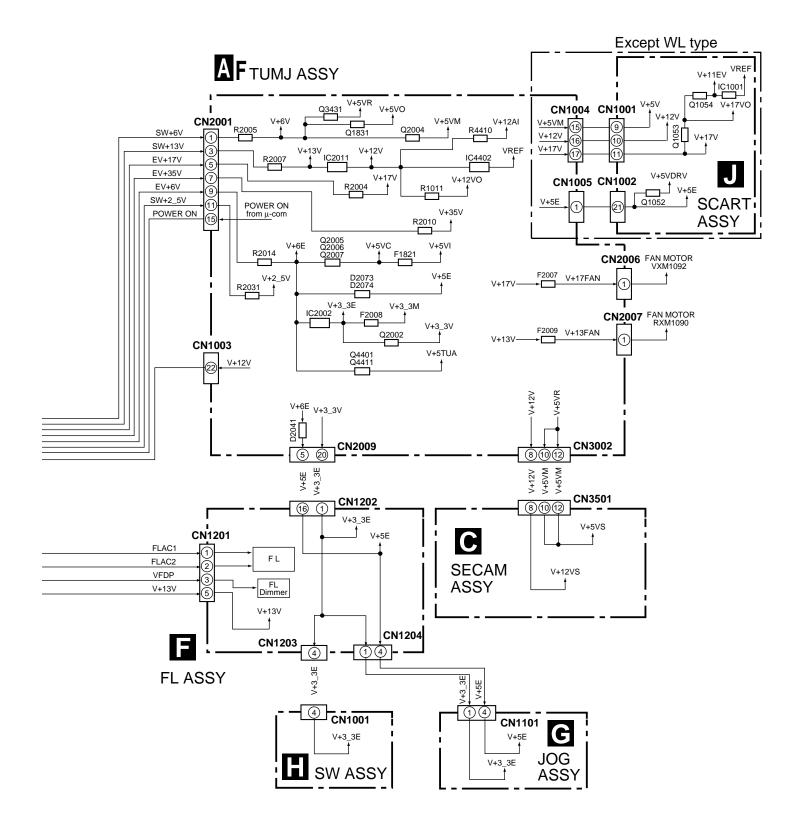
3.1.3 SCART ASSY BLOCK DIAGRAM



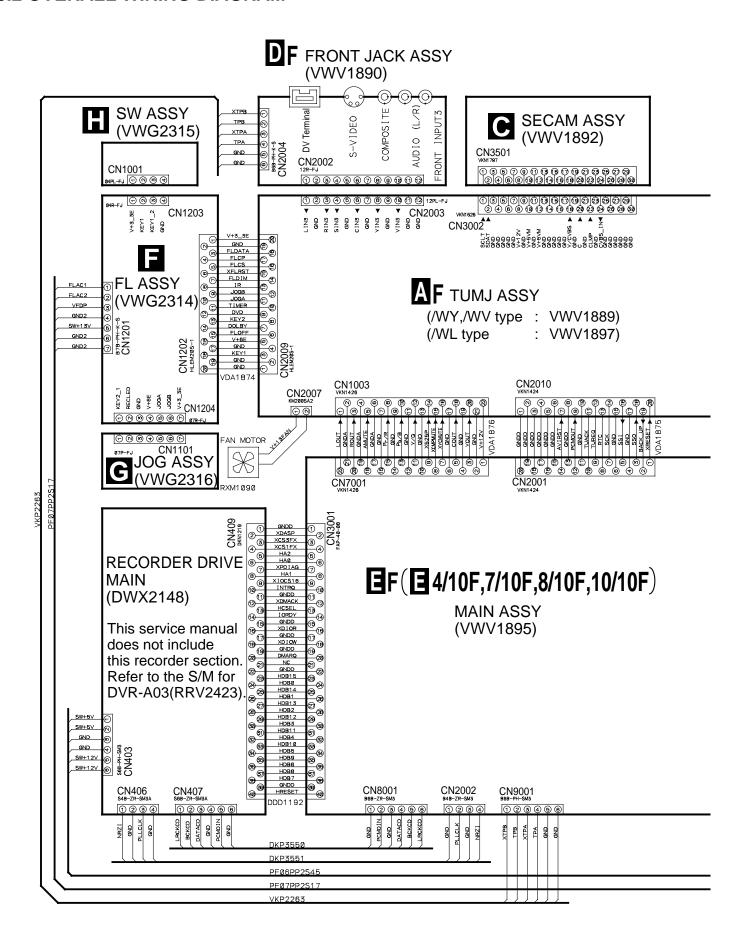


3.1.4 POWER BLOCK DIAGRAM

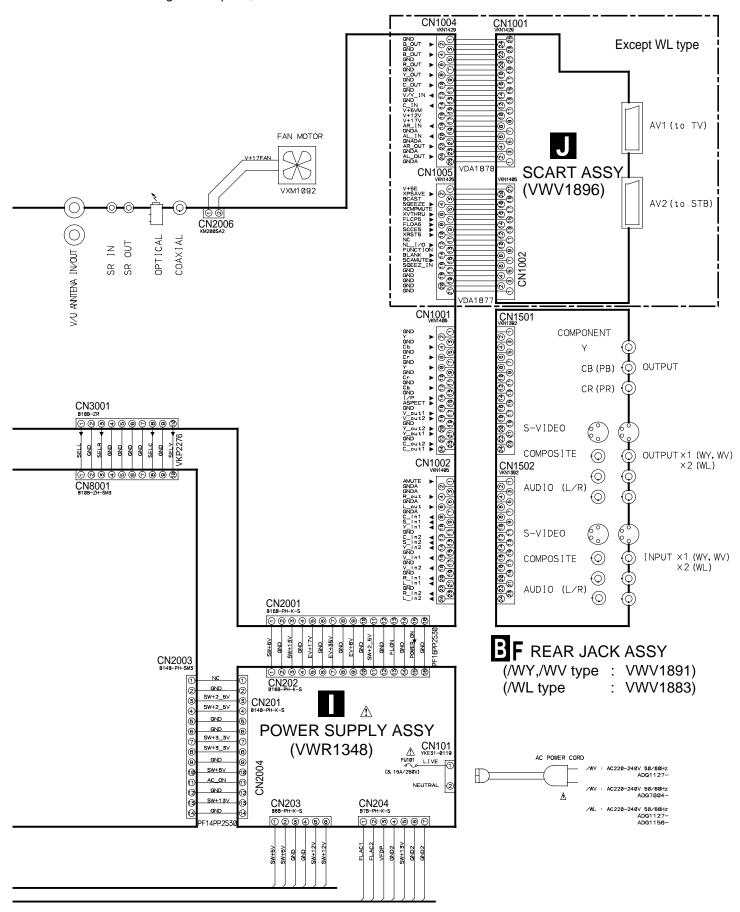




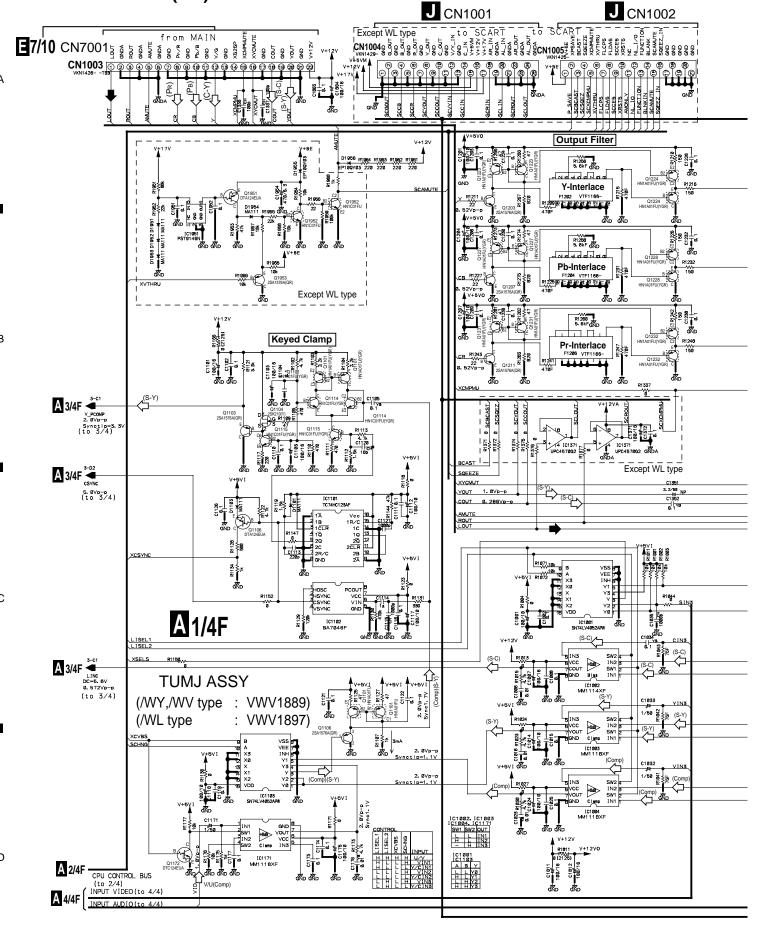
3.2 OVERALL WIRING DIAGRAM



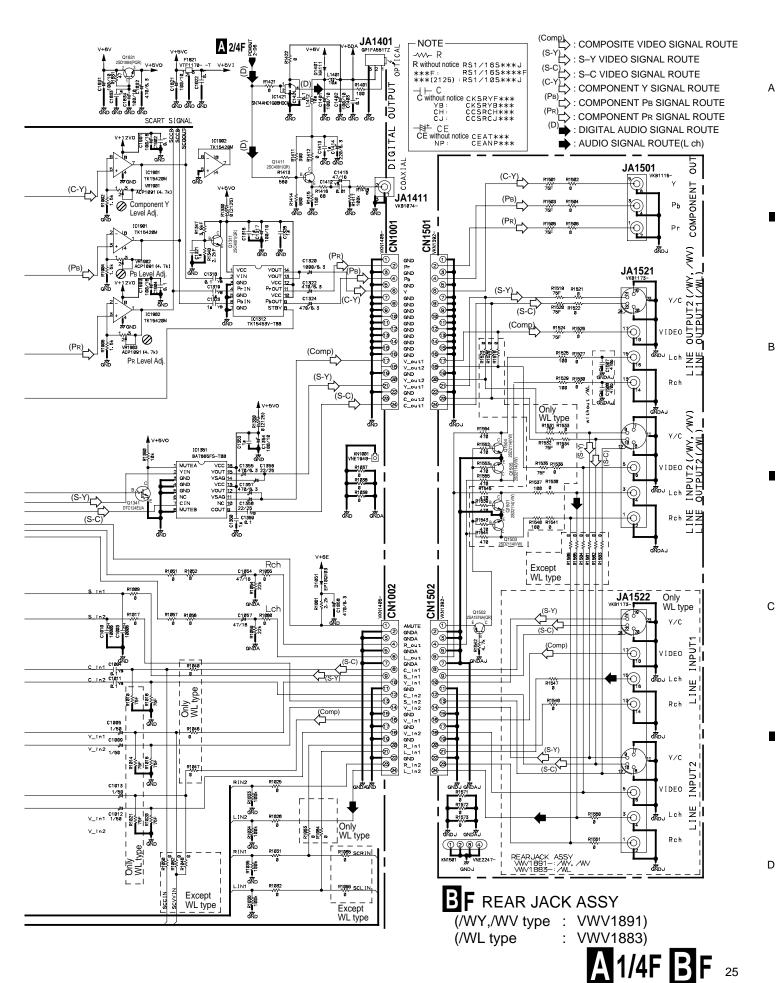
Note: When ordering service parts, be sure to refer to "EXPLODED VIEWS and PARTS LIST" or "PCB PARTS LIST".



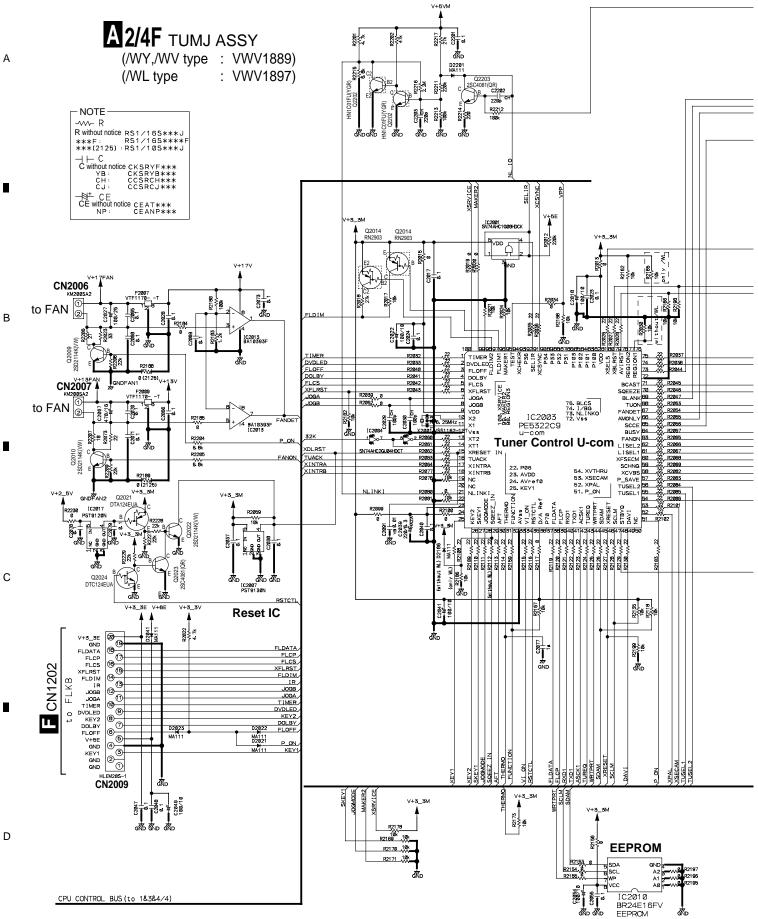
3.3 TUMJ ASSY(1/4) and REAR JACK ASSY



3

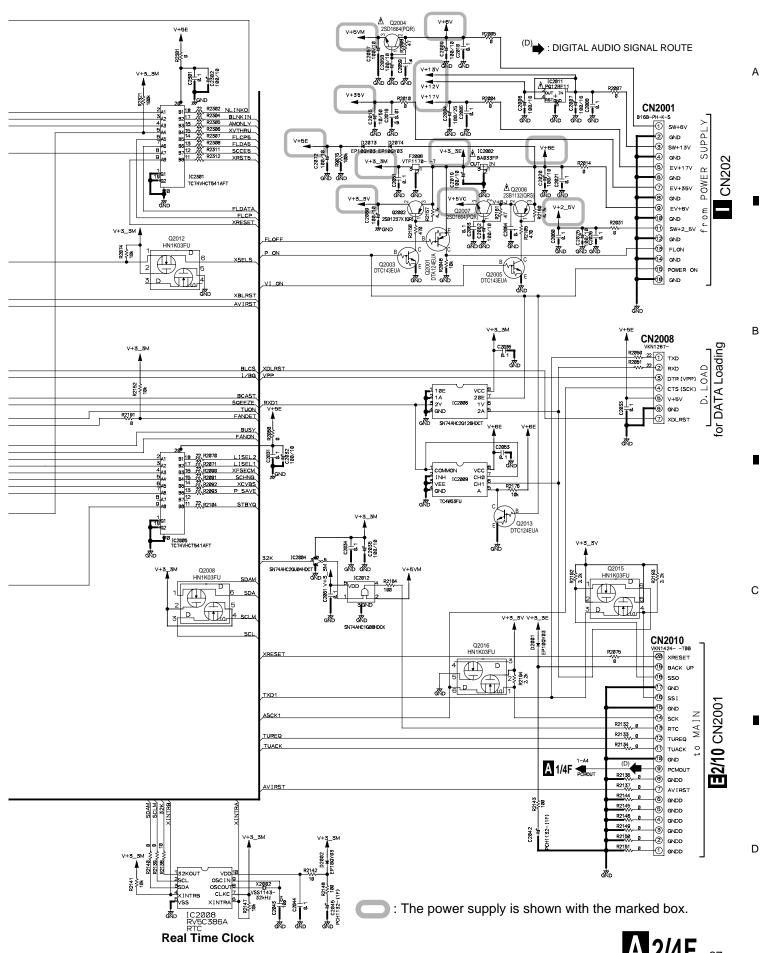


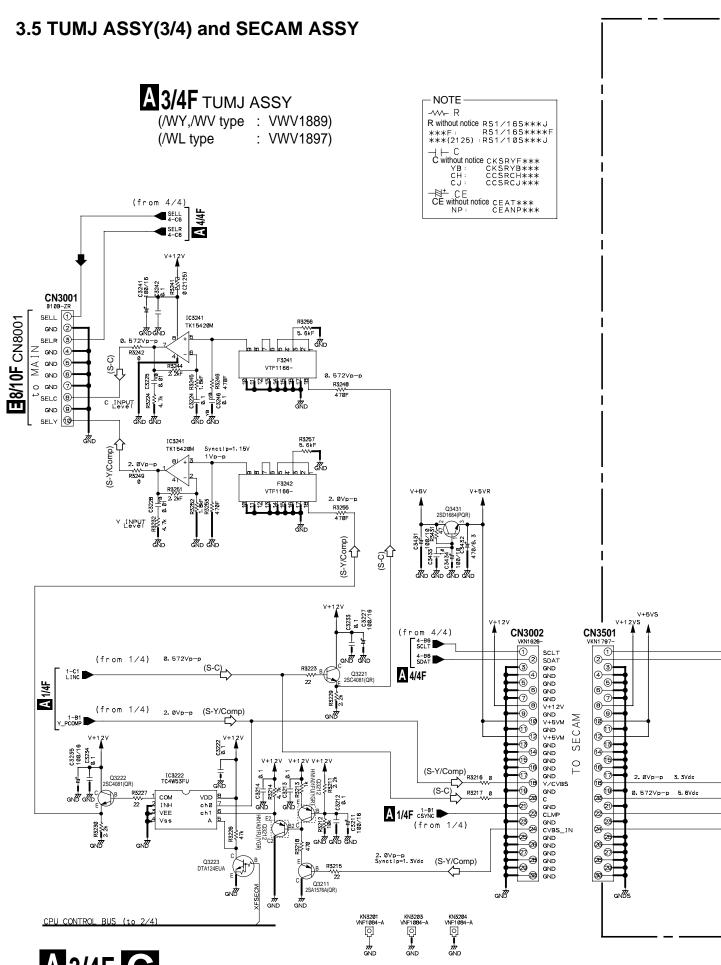
3.4 TUMJ ASSY(2/4)



A 2/4F

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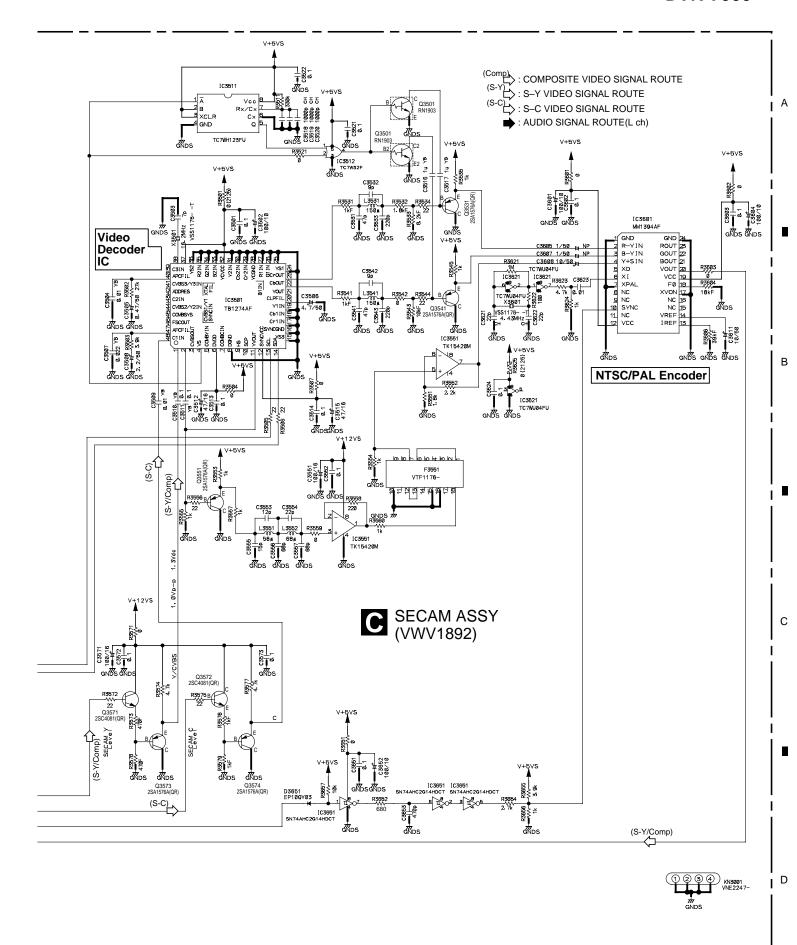


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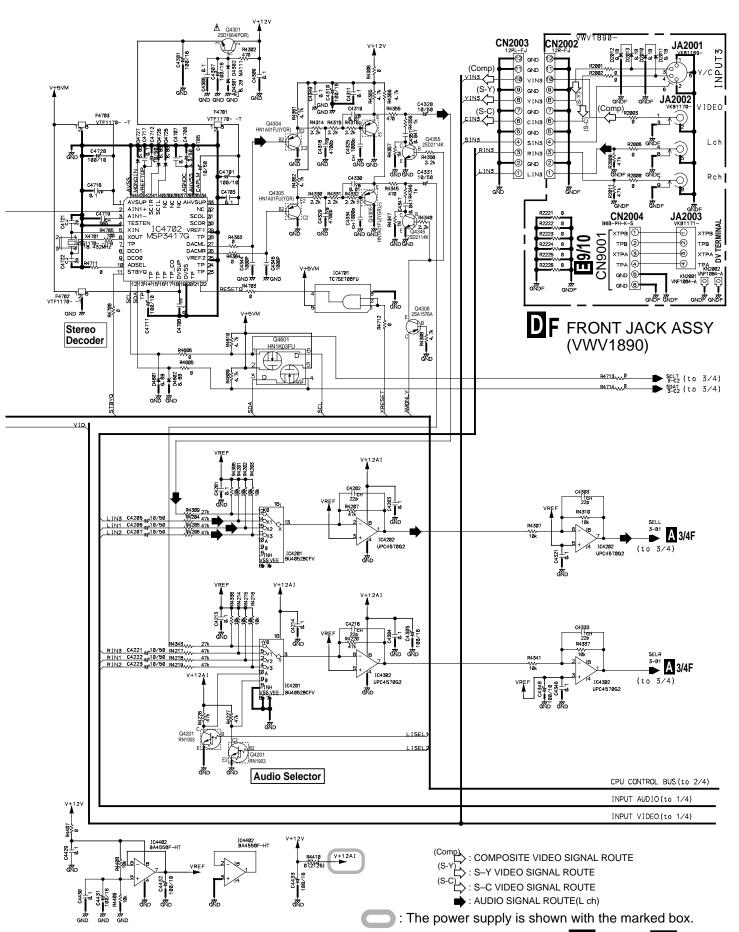
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A 4/4F **D** F

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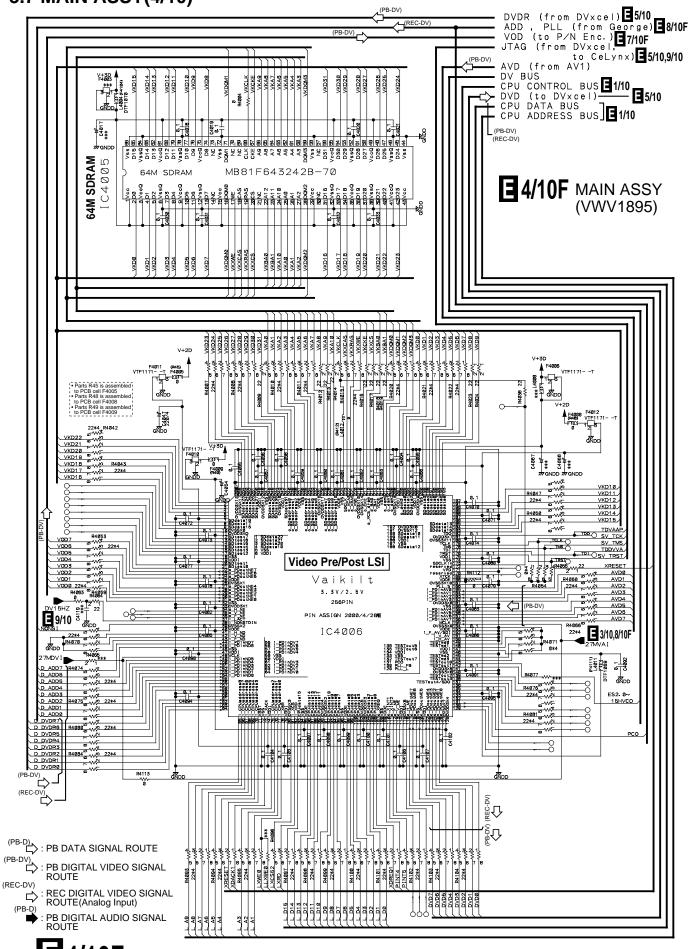
В

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3.7 MAIN ASSY(4/10)

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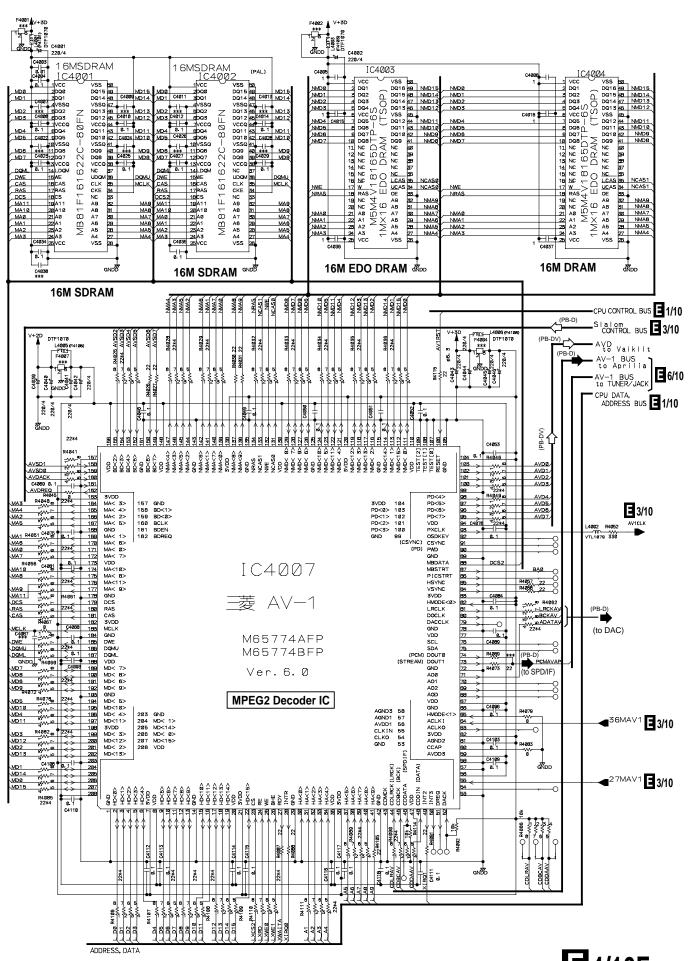


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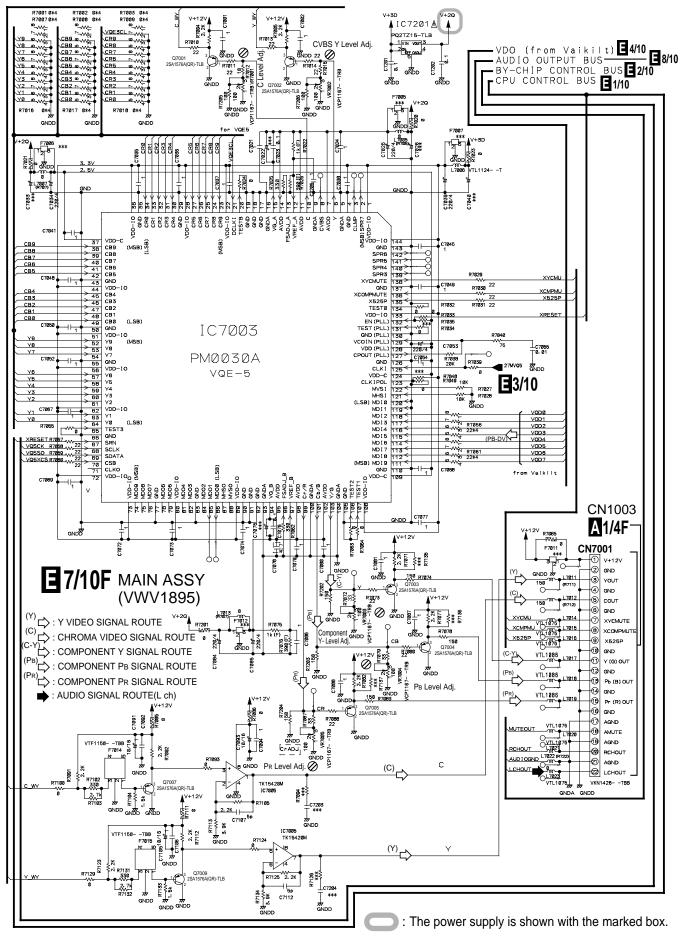
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D/	/R	-7	N	n	N
$oldsymbol{-}$, , ,	•	v	•	u

3.8 MAIN ASSY(7/10)

IC7004 M32L1632512A-8Q and IC7006 PM0024AF is deleted.

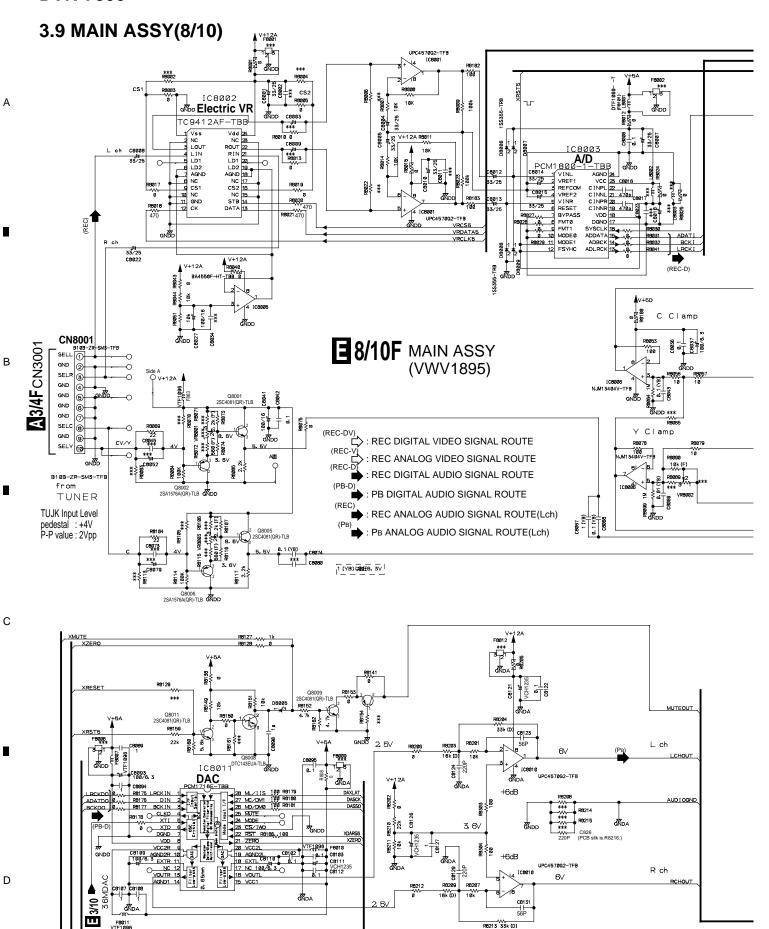


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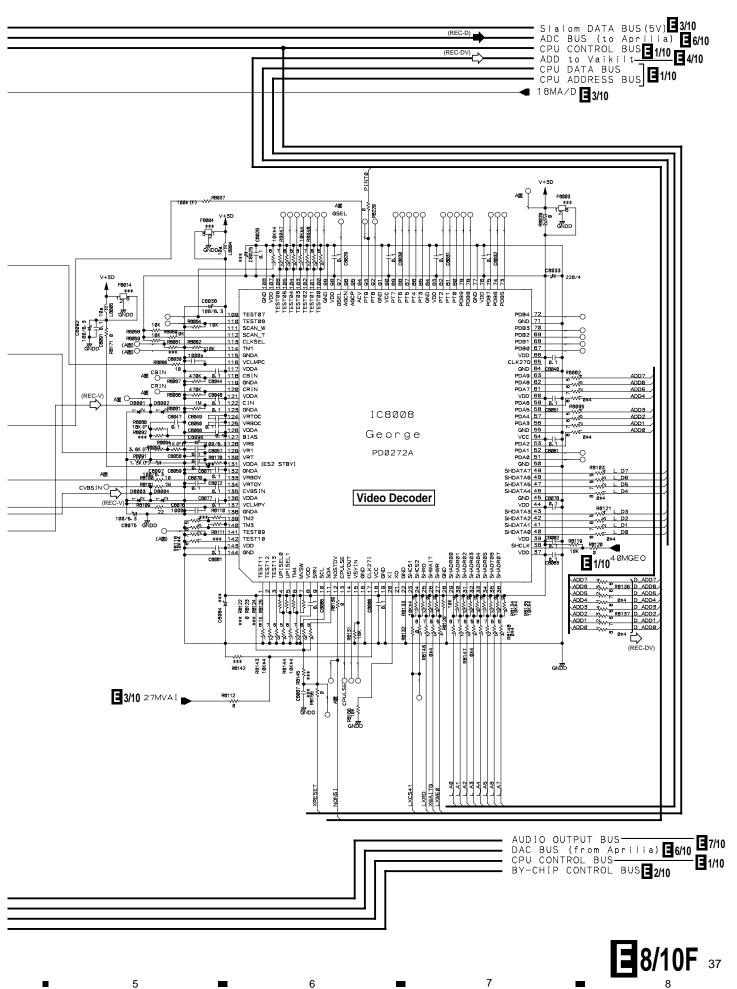
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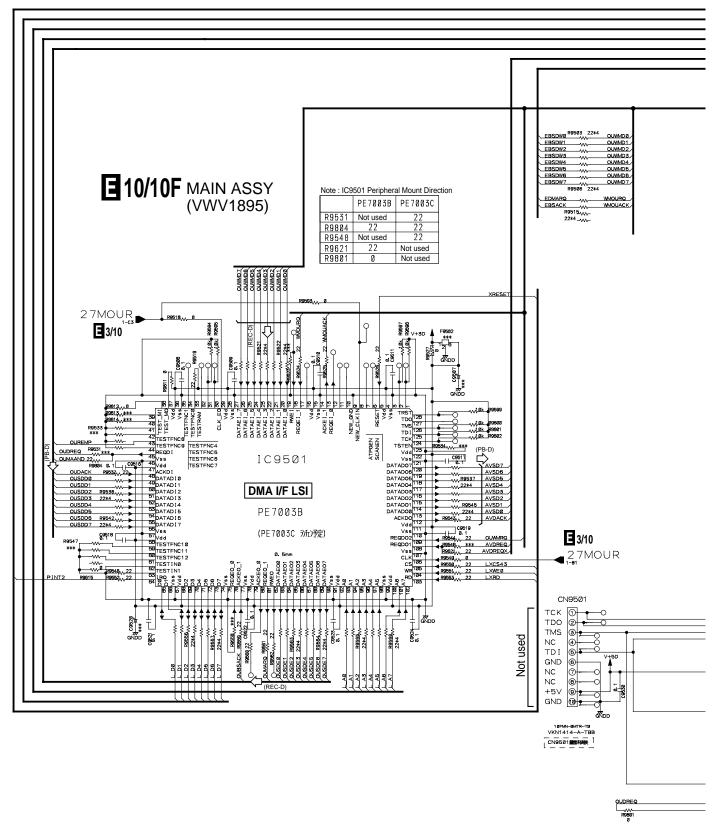
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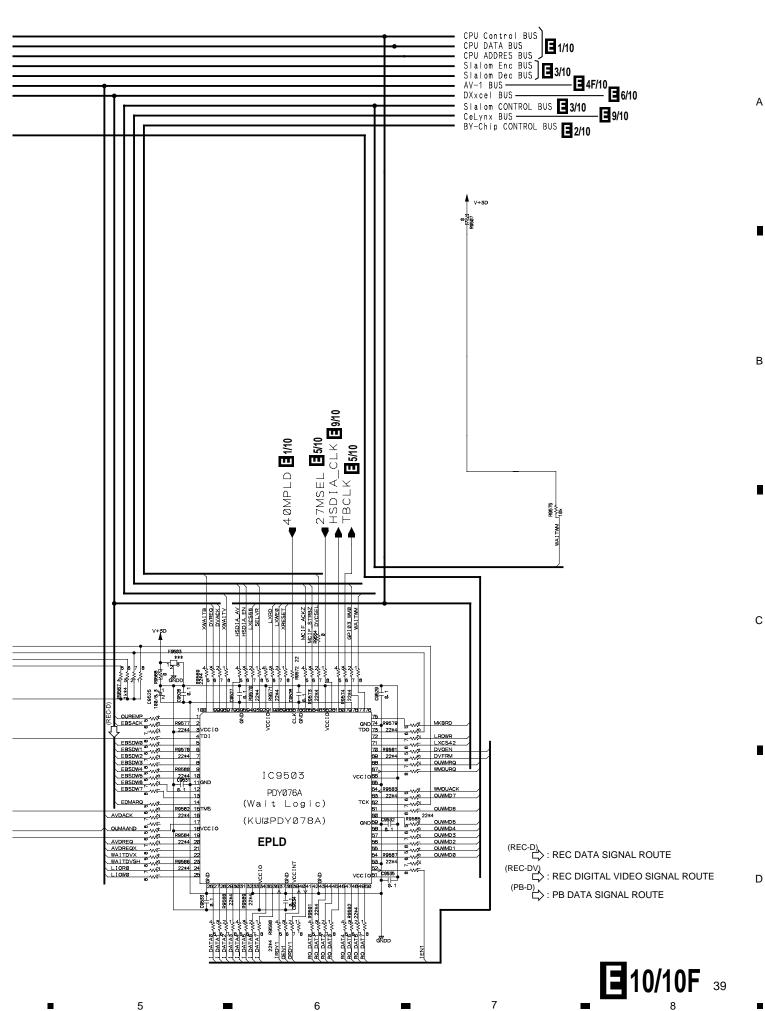
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38 **1**0/10F

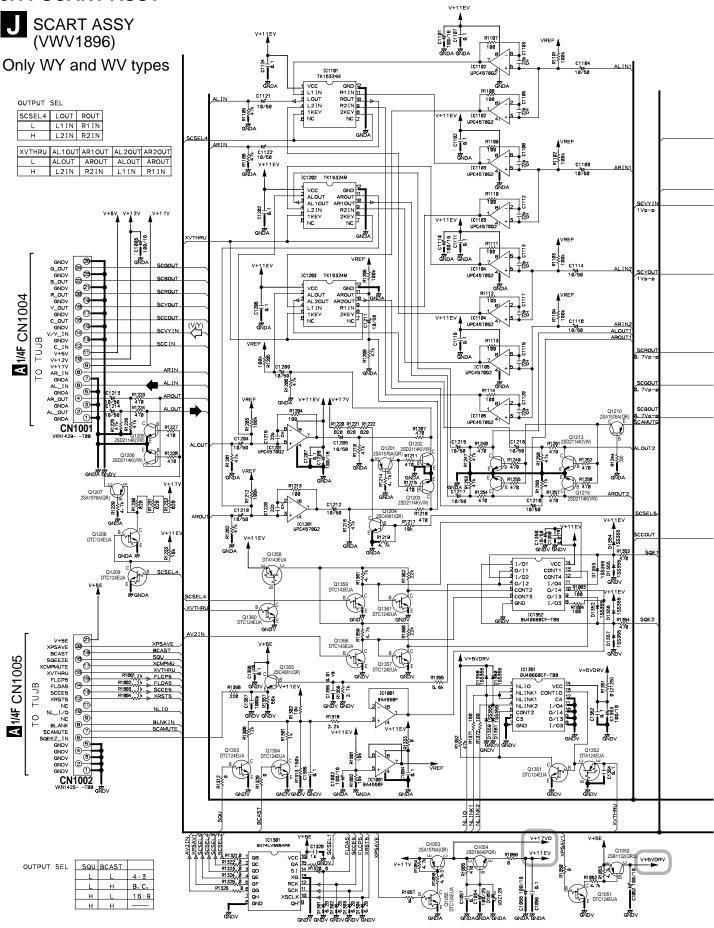
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3.11 SCART ASSY



J

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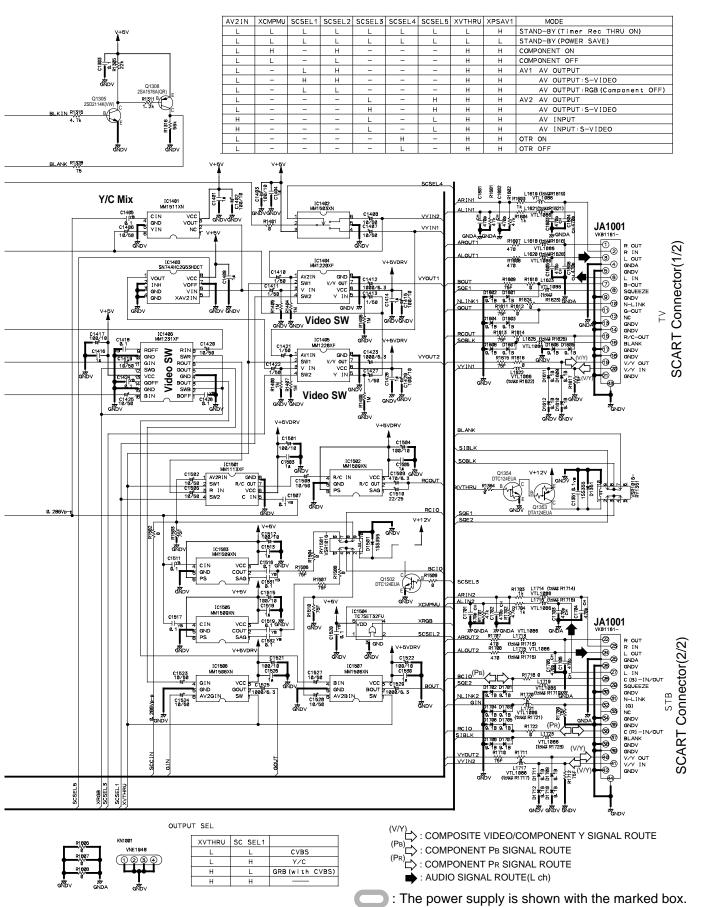
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DVR-7000 4. PCB CONNECTION DIAGRAM 4.1 TUMJ ASSY **C** CN3501 SK2 GND **E** CN1202 GND CN1005 AF TUMJ ASSY (VNP1845-B) J CN1002 CN2001 NOTE FOR PCB DIAGRAMS: 3. The parts mounted on this PCB include all necessary parts for diagrams.

2. A comparison between the main parts of PCB and schematic several destinations. CN8001 For further information for respective destinations, be sure to check with the schematic diagram.
4. View point of PCB diagrams. CN7001 Connector Capacitor SIDE A • <u>6 0 0</u> 0 O S SIDE B P.C.Board Chip Part CN1001 <u>©©©</u> FAN 000 **MOTOR** FAN **MOTOR**

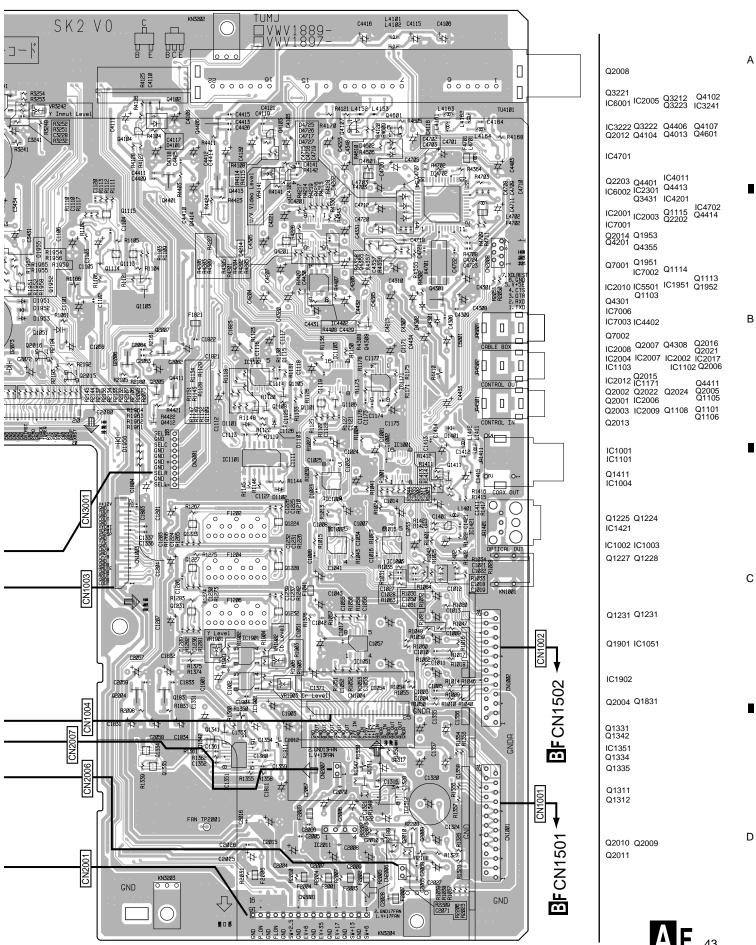
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SIDE A

CN202



DVR-7000

Q4108

Q4161

2

IC4302

Q4345

IC4202

Q8001

Q1172

Q1203

Q1207

Q1211

IC1371

D IC2013

TUMJ □VWV188 0 000 4060 \bigcirc

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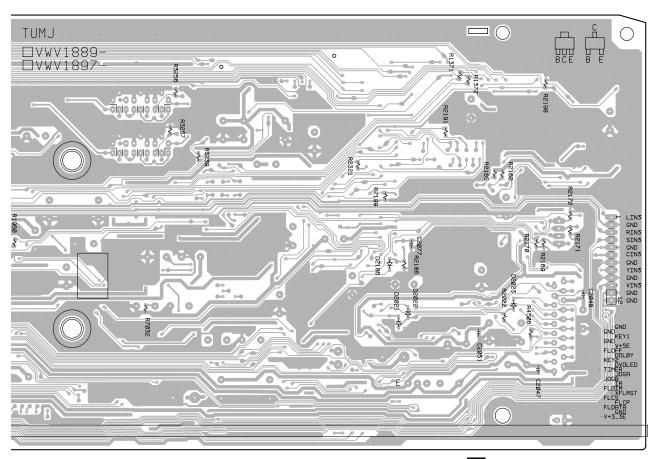
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DVR-7000



5

(VNP1845-B)

AF TUMJ ASSY

SIDE B

A F 45

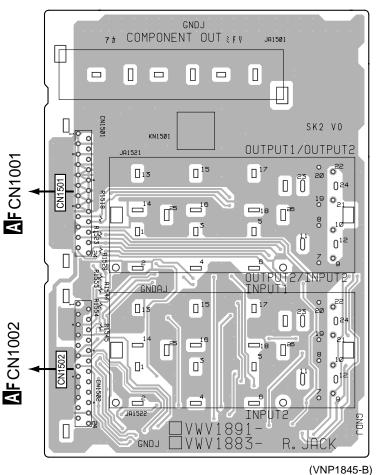
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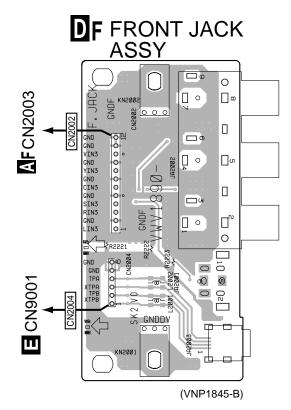
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5

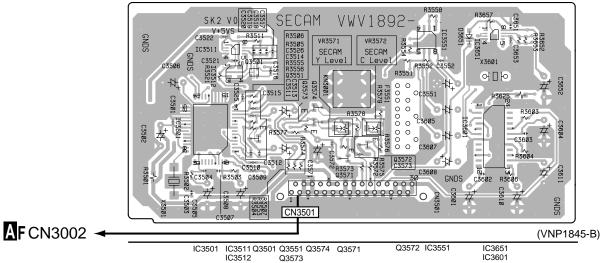
4.2 REAR JACK, SECAM and FRONT JACK ASSYS

BF REAR JACK ASSY





C SECAM ASSY

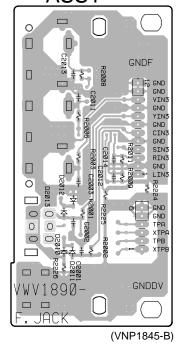




SIDE A

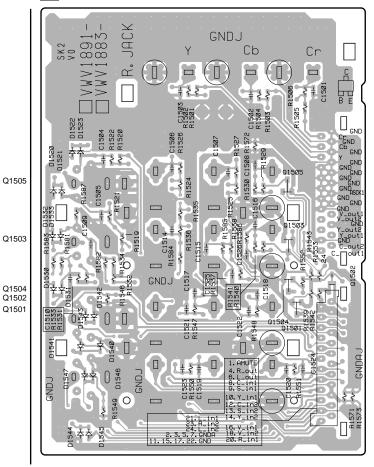
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F FRONT JACK ASSY



B F REAR JACK ASSY

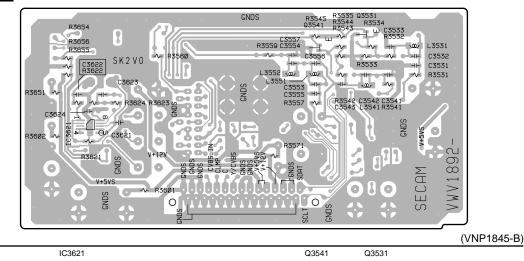
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(VNP1845-B)

С

C SECAM ASSY



SIDE B

4.3 SCART ASSY

AFCN1004 J SCART ASSY VWV1896 SIDE A **AFCN1005** В 00000 (VNP1849-A) Q1210 Q1214 Q1214 IC1405 IC1505 IC1406 IC1403 Q1502 IC1503 IC1401 Q1359 Q1361 Q1358 Q1360 IC1352 Q1357 IC1351 Q1356 Q1351 Q1501 Q1053 Q1055 Q1054 IC1101 IC1202 IC1203 Q1212 Q1213 IC1504 IC1506 IC1301 IC1201 Q1202 Q1203 Q1201 IC1001 Q1304 IC1404 Q1052 Q1051

J

2

■ 3 ■ 4

3

Q1353

5. ADJUSTMENT

5.1 TUMJ ASSY ADJUSTMENT

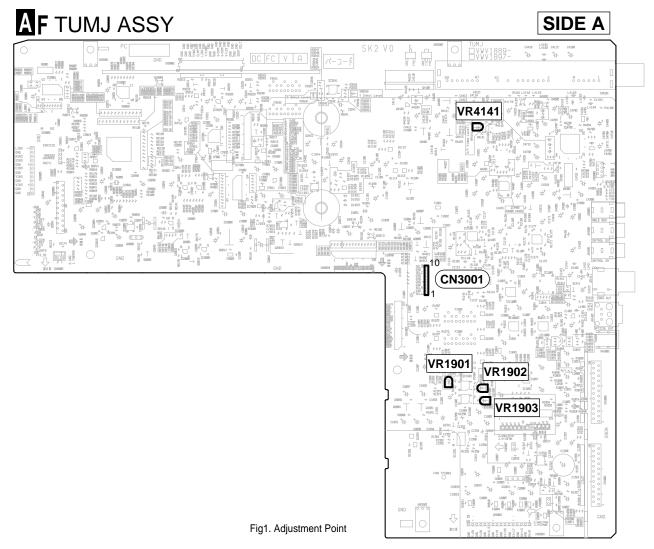
Note: Use disc: [DVD PAL test disc] It is recommended to adjust using PAL disc.

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
1	Video level adjustment of terrestrial wave (Input system adjustment)	VR4141	TUMJ ASSY CN3001 Pin10(SEL Y)	2.00Vp-p ± 100mV	Input a signal of PAL-I/White 100% 70dBµV to terrestrial wave input(21ch=471.25MHz). Adjust after stable thermal characteristic.
2	Y level adjustment of component system (Output system adjustment)	VR1901	Component ouput (Y) (75Ω terminate)	1.0Vp-p ± 40mV	PAL 100% color-bar data playback
3	PB level adjustment of component system (Output system adjustment)	VR1902	Component ouput (PB) (75Ω terminate)	700mVp-p ± 28mV	PAL 100% color-bar data playback
4	PR level adjustment of component system (Output system adjustment)	VR1903	Component ouput (PR) (75Ω terminate)	700mVp-p ± 28mV	PAL 100% color-bar data playback

When NTSC test disc GGV1025 is used, the adjustment No.2 to No.4 value is changed to the following value.

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
	Y level adjustment of component system (Output system adjustment)	VR1901	Component ouput (Y) (75Ω terminate)	980mVp-p ± 39mV	NTSC 75% color-bar data playback
	PB level adjustment of component system (Output system adjustment)	VR1902	Component ouput (PB) (75Ω terminate)	525mVp-p ± 21mV	NTSC 75% color-bar data playback
	PR level adjustment of component system (Output system adjustment)	VR1903	Component ouput (PR) (75Ω terminate)	525mVp-p ± 21mV	NTSC 75% color-bar data playback

Note: Do the MAIN ASSY adjustment first, before TUMJ ASSY adjustment. When using 75% color bar, adjust making PB/PR output to 75%.



5.2 MAIN ASSY ADJUSTMENT

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
1	Master clock free-running adjustment (Clock system adjustment)	VC3001	MAIN ASSY IC4007 Pin54 (CLKO) (M65774AFP)	27.000000MHZ ± 130Hz	No input signal or during test disc play- back
2	Y level adjustment of CVBS system (Output system adjustment)	VR7002	Y output of S terminal (75Ω termination)	1.0Vp-p ± 40mV	Playback the PAL DVD test disc(100% color-bar). Terminate the Y output of S terminal with 75Ω and adjust so that the level of between sync tip and white peak becomes 1.0Vp-p.
3	C level adjustment of CVBS system (Output system adjustment)	VR7001	C output of S terminal (75Ω termination)	300mVp-p ± 12mV	Playback the PAL DVD test disc(100%colorbar). Terminate the C output of S terminal with 75Ω and adjust so that the amplitude of color burst becomes 300mVp-p.
4	Y level adjustment of component system (Output system adjustment)	VR7003	MAIN ASSY CN7001 Pin11 (Y(G) Out)	760mVp-p ± 22mV	Playback the PAL DVD test disc(100% color-bar). At the pin 11 of CN7001 in the MAIN ASSY, adjust so that the level of between sync tip and white peak becomes 760mVp-p.
5	PB level adjustment of component system (Output system adjustment)	VR7004	MAIN ASSY CN7001 Pin13 (PB(B) Out)	520mVp-p ± 15mV	Playback the PAL DVD test disc(100%colorbar). At the pin 13 of CN7001 in the MAIN ASSY, adjust so that the level of between bottom and top becomes 520mVp-p in the 100% color-bar screen.
6	PR level adjustment of component system (Output system adjustment)	VR7005	MAIN ASSY CN7001 Pin15 (PR(R) Out)	520mVp-p ± 15mV	Playback the PAL DVD test disc(100%colorbar). At the pin 15 of CN7001 in the MAIN ASSY, adjust so that the level of between bottom and top becomes 520mVp-p in the 100% color-bar screen.

When NTSC test disc GGV1025 is used, the adjustment No.2 to No.6 value is changed to the following value.

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
2	Y level adjustment of CVBS system (Output system adjustment)	VR7002	Y output of S terminal (75Ω termination)	980mVp-p ± 39mV	Playback the NTSC DVD test disc (75% color-bar). Terminate the Y output of S terminal with 75Ω and adjust so that the level of between sync tip and white peak becomes 980mVp-p .
3	C level adjustment of CVBS system (Output system adjustment)	VR7001	C output of S terminal (75Ω termination)	280mVp-p ± 11mV	Playback the NTSC DVD test disc(75%colorbar). Terminate the C output of S terminal with 75Ω and adjust so that the amplitude of color burst becomes 280mVp-p.
4	Y level adjustment of component system (Output system adjustment)	VR7003	MAIN ASSY CN7001 Pin11 (Y(G) Out)	745mVp-p ± 22mV	Playback the NTSC DVD test disc (75% color-bar). At the pin 11 of CN7001 in the MAIN ASSY, adjust so that the level of between sync tip and white peak becomes 745mVp-p.
5	PB level adjustment of component system (Output system adjustment)	VR7004	MAIN ASSY CN7001 Pin13 (PB(B) Out)	390mVp-p ± 12mV	Playback the NTSC DVD test disc(75%colorbar). At the pin 13 of CN7001 in the MAIN ASSY, adjust so that the level of between bottom and top becomes 390mVp-p in the 75% color-bar screen.
6	PR level adjustment of component system (Output system adjustment)	VR7005	MAIN ASSY CN7001 Pin15 (PR(R) Out)	390mVp-p ± 12mV	Playback the NTSC DVD test disc (75% color- bar). At the pin 15 of CN7001 in the MAIN ASSY, adjust so that the level of between bottom and top becomes 390mVp-p in the 75% color-bar screen.

Note: Do the MAIN ASSY adjustment first, before TUMJ ASSY adjustment.

When using 75% color bar, adjust making PB/PR output to 75%.

EF MAIN ASSY

SIDE A

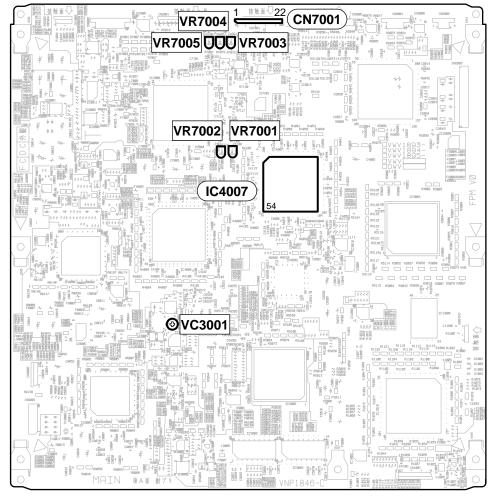


Fig.2 Adjustment Point

6. GENERAL INFORMATION

6.1 MODEL TYPE AND REGION SETTING

■ Setting the Model type and Region No. for DVD Recorder

For the DVD recorder DVR-7000/WY,/WV and /WL, it is necessary to set the region No. [2 or 3] on the FLASH ROM in the MAIN ASSY and the model type [WY,WV and WL] on the EEPROM in the TUMJ ASSY. So when the MAIN ASSY or TUMJ ASSY is renewed, "The Model type and Region setting mode screen" is displayed automatically.

Note: If the region No. is once set, it is unable to rewrite it. When it is necessary to change the region No., renew the MAIN ASSY. And it is able to rewrite the once set model type on the EEPROM in the TUMJ ASSY only when the MAIN ASSY is renewed and setting the new region No. on the FLASH ROM.

• How to set the Model type and Region No.

- 1. Turn the power on.
- The setting request screen is displayed when the model type and region No. is not set. At this time FL displays " MODE SETTING".

/WY,/WV [Recorder's Model and Region Setting] Please pick out any one of the following.

Button No. Model Region [1 : WY_MODEL<Europe> Region 2] [2 : WV_MODEL<UK> Region 2]

/WL [Recorder's Model and Region Setting] Please pick out any one of the following.
Button No. Model Region
[3 : WL_MODEL<Hong Kong> Region 3]

- 3. Enter the data according to the mode menu by the service remote control unit.
- 4. The recorder restarts automatically.
- Set the shipping position. (stop + power off)
 But it is omitted when making the Down Load of the system μ-com is done after this.
- 6. Turn off the power, then turn on the power again.

● When the FL displays "MODEL MISMATCH" after connecting the AC plug to the outlet.

It displays, connecting the AC plug to the outlet when the setting is mismatched between the software setting of the model type data on the EEPROM and the μ -com hardware pin setting of the model type in the TUMJ ASSY. At this time, it is unable to turn on the power.

It is considered the TUMJ PCB board fault (model type hardware pin setting fault).

Note: [Tuner control μ-com hardware pin setting of the model type] Pin 76=Region 1, Pin 77=Region 2, Pin 98=Region 3

Check the corresponded pin according to the right table. L: Pull down H: Pull up

Tuner μ-com Hardware Pin Setting Table

Pin76 Pin77 Pin98

WY, WV type L H L

WL type H H L

• When the screen shows the following display after turning on the power

<display 1>
< Model and Region don't match > Model [already memorized on the TUFL-EEPROM]: WY_MODE | Region [already memorized on the MAIN-CPU-FLASH ROM]: region in Please take the power-plug off the plug socket
[When WL type Materials or the plug socket]

.... model type information in the TUMJ ASSY

· region information memorized in the MAIN ASSY

[When WL type MAIN Board is mounted to the WY type model.]

It displays, exchanging the MAIN ASSY or TUMJ ASSY, etc when the combination of model type and region No. already set is mismatched.

After this, it is unable to operate any functions.

Match the combination between the model type and region No. setting, or renew the ASSY and set the data newly.

■ When the screen shows the following display after setting the Model type and Region No.

<display 2>
< You can't change and overwrite the Region No. ! > Region was already memorized on the MAIN-CPU-FLASHROM and you can't overwrite the different Region.
Region[already memorized on the MAIN-CPU-FLASHROM] 3
Model-Region[that you selected just now] WY_MODEL -2.
Please take the power-plug off the plug socket.

region information memorized in the MAIN ASSY

region information selected by the key input at the setting mode screen

[When WY type TUMJ Board is is paired to the WL type MAIN Board.]

It displays, renewing TUMJ ASSY, etc when setting the different model type from the region No. already set in the FLASH ROM in the MAIN ASSY.

Match the combination between the model type and region No. setting, or renew the MAIN ASSY and set the data newly.

6.2 IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

• List of IC

PE5322C9, MSP3417G, LC749793JM, TB1274AF, MM1394AF, MM1511XN, MM1228XF, MM1231XN

■ PE5322C9 (TUJB ASSY : IC2003)

• Tuner Control Microcomputer

• Pin Function (1/2)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
1	P120	TIMER	0	LED for timer	41	P21	TXD1	0	MAIN communication line
2	P121	DVDLED	0	DVDLED	42	P22	ASCK1	ı	WAIN COMMUNICATION INTE
3	P122	FLOFF	0	For FL OFF	43	P23	TUREQ	0	Communication request of tuner control IC
4	P123	DOLBY	0	LED for FL DOLBY	44	P24	WRTPRT	0	EEPROM writing permission
5	P124	FLCS	0	FL Driver communication line	45	P25	SDAM	I/O	I2C data input/output
6	P125	XFLRST	0	FL DRIVE reset signal	46	P26	XRESET	0	RESET OUT
7	P126	JOGA	ı	FL JOG input	47	P27	SCLM	0	I2C clock input
8	P127	JOGB	ı	FL JOG input	48	P80	STBYQ	0	Audio demultiplex standby mode
9	VDD	VDD	_	Power supply	49	P81	XDAVI	I	"L" when PDC data is ready
10	X2	X2	١,	Connect a 6MHz ceralock	50	P82	NC	_	NC
11	X1	X1	'	Connect a divil 12 ceralock	51	P83	P_ON	0	POWER ON signal
12	Vss	Vss	_	Ground	52	P84	XPAL	0	L:PAL, H:SECAM
13	XT2	XT2		32k input	53	P85	XSECAML	0	L:SECAML, H:SECAML'
14	XT1	XT1		0_10 11 p 000	54	P86	XVTHRU	0	Scart L : Scart through
15	XRESET	XRESETIN	I	Reset IC input	55	P87	TUSEL1	0	Select the ground wave or BS
16	P00	TUACK	ı	MAIN communication line	56	P40	TUSEL2		Select the ground wave or BS
17	P01	XINTRA		RTC communication	57	P41	P_SAVE	0	Scart save power mode
18	P02	XINTRB		TVTO communication	58	P42	XCVBS	0	S composite select
19	P03	NC	_	NC	59	P43	SCHNG	0	S-input select signal for PAL model
20	P04	NC	_	NC	60	P44	X4L	0	4-line Y/C separation for PAL
21	P05	NLINKI	I	NLINK data input	61	P45	LINSEL1	0	External input switch 1
22	P06	NC	_	NC	62	P46	LINSEL2	0	External input switch 2
23	AVdd	AVdd	_	Power supply	63	P47	F_ON	0	ON/OFF signal for fan
24	AVRef0	A/D Ref	ı	A/D reference voltage input	64	P50	BUSY	I	Braster BUSY signal
25	P10	KEY1		FL KEY input 1	65	P51	SCCE	0	Scart Boad serial-parallel enable
26	P11	KEY2		FL KEY input 2	66	P52	NC	_	NC
27	P12	NC		NC	67	P53	FANDET	I	FAN rotation detection
28	P13	INC	_	INC .	68	P54	TUON	0	Tuner ON
29	P14	FUNCTION	I	Scart function input (STBY)	69	P55	BLANK	I	Scart Blanking signal
30	P15	AFT	ı	Ground wave tuning gap input	70	P56	SQEEZE	0	SQEEZE signal for D terminal and Scart
31	P16	THERMO	ı	Temperature detection input	71	P57	LET_S	0	LETTER signal for S terminal
32	P17	NC	_	NC	72	Vss	Vss	_	Ground
33	Avss	Avss	_	Analog ground	73	P60	NLINKO	0	N Link output signal for Scart
34	P130	VI_ON	0	Video circuit ON for LINE input	74	P61	NC	_	NC
35	P131	RSTCTL	0	Reset mute signal for sag measures	75	P62	BLCS	0	Chip select signal for braster
36	AVRef1	D/A Ref	I	D/A reference voltage input	76	P63	REGION1		Region 1
37	P70				77	P64	REGION2	ı	Region 2
38	P71	FLDATA		EL DDIVED communication !	78	P65	AV1RST	0	AV1 reset signal
39	P72	FLCP	0	FL DRIVER communication line	79	P66	XBLRST	0	Braster reset signal
40	P20	RXD1	ı	MAIN communication line	80	P67	XSELCS	I	For S input detection/for S signal switch (EU)

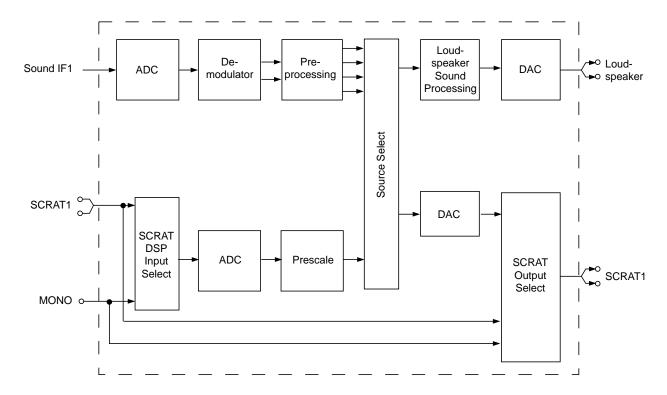
• Pin Function (2/2)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	1/0	Pin Function
81	VDD	VDD	_	Power supply	91	P35	SELIR	I	Remote control input
82	P100				92	P36			
83	P101				93	P37	XCHEKR	I	Checker mode
84	P102				94	TEST	VPP	I	VPP input for FLASH
85	P103				95	P90	MAKER1	ı	Manufacture identification code 1
86	P30				96	P91	FLDIM1	0	For FLDIMER
87	P31				97	P92	FLDIM2		FOI FLOIMER
88	P32				98	P93	REGION3	I	Destination code 3
89	P33				99	P94	MAKER2	ı	Manufacture identification code 2
90	P34	CSSYNC	I	CSSYNC input for CSREC	100	P95	XSRVICE	Ι	Service mode

■ MSP3417G (TUJB ASSY : IC4702)

• Stereo Decoder IC

Block Diagram



• Pin Function

Pin No. PMQFP 44-pin	Pin Name	Туре	Connection (it not used)	Descriptiom
1	AVSUP		Х	Analog power supply
2	ANA_IN1+	IN	LV	IF input1
3	ANA_IN-	IN	LV	IF common
4	TESTEN	IN	Х	Test pin
5	XTAL_IN	IN	Х	Crystal oscillator
6	XTAL_OUT	OUT	Х	Crystal oscillator
7	TP		LV	Test pin
8	D_CTR_I/O_1	IN/OUT	Х	D_CTR_I/O_1
9	D_CTR_I/O_0	IN/OUT	Х	D_CTR_I/O_0
10	ADR_SEL	IN	Х	I2C Bus address select
11	STANDBYQ	IN	Х	Standby(low-active)
12	I2C_CL	IN/OUT	Х	IIC clock
13	I2C_DA	IN/OUT	Х	IIC data
14	TP		LV	Test pin
15	TP		LV	Test pin
16	TP		LV	Test pin
17	TP		LV	Test pin
18	TC_PO	OUT	LV	Test pin*
19	DVSUP		Х	Digital power supply+5V
20	DVSS		Х	Digital ground
21	TP		LV	Test pin
22	RESETQ	IN	Х	Power-on-reset
23	NC		LV	Not connected
24	NC		LV	Not connected
25	VREF2		Х	Reference ground 2 high-voltage part
26	DACM_R	OUT	LV	Loudspeaker out, right
27	DACM_L	OUT	LV	Loudspeaker out, left
28	NC		LV	Not connected
29	VREF1		Х	Reference ground 1 high-voltage part
30	SC1_OUT_R	OUT	LV	SCRAT 1 output, right
31	SC1_OUT_L	OUT	LV	SCRAT 1 output, left
32	NC		LV	Not connected
33	AHVSUP		Х	Analog power supply + 8.0 V
34	CAPL_M		Х	Volume capacitor MAIN
35	AHVSS		Х	Analog ground
36	AGNDC		Х	Analog reference voltage high-volt-age part
37	NC		LV	Not connected
38	NC		LV	Not connected
39	NC		LV	Not connected
40	SC1_IN_L	IN	LV	SCRAT 1 input, left
41	SC1_IN_R	IN	LV	SCRAT 1 input, right
42	VREFTOP		Х	Reference voltage IF A/D converter
43	MONO_IN	IN	LV	Mono input
44	AVSS		Х	Analog ground

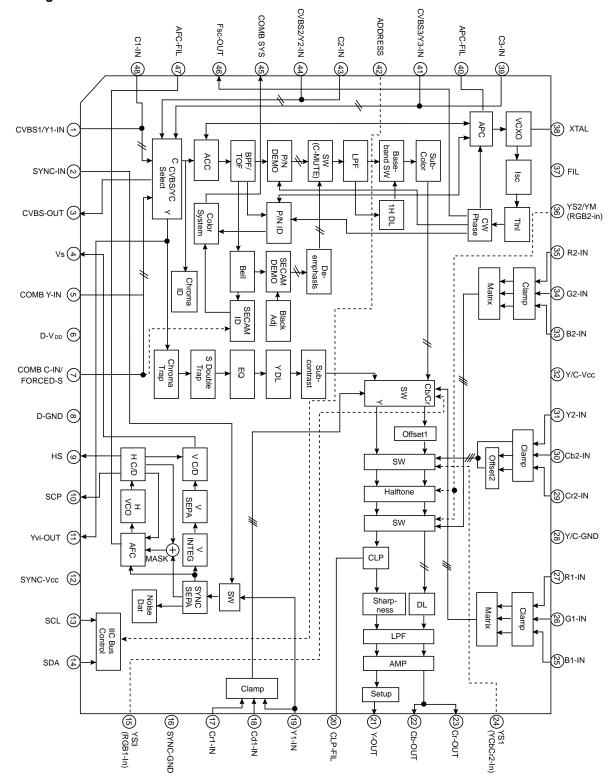
■ LC74793JM (TUJB ASSY : IC7001) • VPS, PDC, Data Slicer IC ₽ST CDLR • Block Diagram CTRL1 Timing generator) X ∏ × Vout HOUT AFC circuit (VCO) Data loading circuit VCOR VCO in C Pout Synchronous identification circuit Data latch circuit V separation circuit SYNCJDG Synchronous separation data separation circuit Interface SEP OUT □ SYNIN SDA VDD1,2 SEPC VDD1,2 SCL SEP IN CTRL2

• Pin Function

Pin No.	Pin No.	Pin Name	Fuction descriptions
1	VSSI	Ground pin	GND ground pin
2	X train	Xtal Oscillator pin	Pin for connection of a crystal pf Xtal oscillator and capacitor or for input of the external clock (4fsc or 2fsc or fsc)
3	X talout	Xtal Oscillator pin	Pin for connection of a crystal pf Xtal oscillator and capacitor or for input of the external clock (4fsc or 2fsc or fsc)
4	CTRL1	X tal oscillation	Pin of changeover between the external clock input mode and Xtal osillation mode. "Lo"= Xtal oscillation, "Hi"= external clock input
5	- NC -		
6	SDA	IIC Data I/O pins	PDC/VPS data I/O pin IIC bus Write address [0111 1100] IIC bus Read address [0111 1101]
7	SCL	IIC Clock input pin	PDC/VPS data clock inut pin IIC bus
8	SYNCJDG	External synchronous signal identification out put pin	Pin to output the state identified to be with or without the external synchronous signal. "Hi" output for a state with the synchronous signal Xtal oscillation clock out put when RST pin = "Lo" (Not output when reset with the command)
9	Hout	Horizonal synchronous signal output pin	Pin to output the horizonal synchronous signal
10	VSS2	Ground pin	GND ground pin (GND pin for VCO)
11	CP OUT	Charge pump output	For connection of the charge pump output LPF
12	VCOIN	Oscillation control voltage input	VCO oscillation control vortage input pin
13	VCOR	Oscillation control voltage pin	Pin to connect to VCO oscillation range control resister
14	DAV	Data loading output	"Lo" output when the PDC/VPS data is identified
15	VDD2	Power supply pin (+5V)	Power supply pin (+5V : Power supply for VCO)
16	SYNin	Synchronous separation cicuit input pin	Video signal input of the built-in synchronous separation circuit
17	SEPC	Slice level output pin	Slice level check pin
18	SEPOUT	Composite synchronous signal output pin	Pin to output the composite synchronous signal of the built-in synchronous separation circuit
19	SEPIN	Vertical synchronous signal input pin	Pin to input the vertical synchronous signal after integration of the output signal of SEP out pin. Connect the integrating circuit between SEP out pins.Fix this to CDD1 when not using. (Effective with CTRL2 "Hi")
20	Vout	Vertical synchronous signal output pin	Pin to output the vertical synchronous singal. CVO clock output when the RST pin = "Lo" (Not output when reset with the command)
21	CTRL2	SEPin input controp pin	Pin to control whether or not the VSYNC signal is input to SEPin input "Lo" = VSYNC input (Built-in V separation circuit) "Hi" = VSYNC input
22	CDLR	Clock phase control pin	Pin to connect to the clock phase control resister
23	RST	Reset input pin	System reset input pin . Pull-up resistor incorporaited. (Hysteresis input)
24	VDD1	Power supply pin (+5V)	Power supply pin (+5V : digital power supply)

■ TB1274AF (SECAM ASSY : IC3501)

- Video Decoder IC
- Block Diagram



• Pin Function(1/2)

Pin No.	Pin Name	Function	IN/OUT SIGNAL
1	CVBS1/Y1-IN	Input CVBS2 or Y1 signal via clamp C.	CVBS : 1Vp-p Y : 1Vp-p (with sync) DC : 1.8V
2	SYNC-IN	Inputsync signa via clamp C.	1Vp-p (with sync) DC: 1.7V
3	CVBS-OUT	Output terminal for CVBS or Y+C signal	2Vp-p (with sync) DC: 0.6V
4	Vs	Output count_down H sync. Active Hogh	4.7V † High † 5.2V 0V † Low † 0.8V
5	COMB Y-IN	Input Y signal from comb filter via clamp C	1Vp-p (with sync) DC: 1.8V
6	D-VDD	VDD for DDS/BUS/V-CD/H-CD Block	DC 5V
7	COMB C-IN/FORCED-S	IInput C signal from comb filter via clamp C	3Vp-p (burst) DC : 2.4V 4.0V † FORCED-S † 5.0V (Th : 3.5V)
8	D-GND	GND for DDS/BUS/V-CD/H-CD Block	
9	HS	Output H sync with H-AFC. Active Hish	3.8V † High † 4.6V 0 † Low † 1.0V
10	SCP	Output sandcastle pulse. H-BLK pulse with clamp pulse	3.6V † CP † 4.4V 6V † H-BLK † 2.4V 0.0V † Low † 0.8V with pull-down resistor (7.5 k‰)
11	Yvi-OUT	Output Y signal for synchronization selected by Video-SW	1Vp-p (with sync) DC: 2.1V
12	SYNC-Vcc	VCC for SYNC/HVCO block	DC 5V
13	SCL	SCL terminal for IIC bus.	
14	SDA	SDA terminal for IIC bus	
15	YS3 (RGB1-in)	Selection SW for main signal and RGB1 input signal	1.0V † RGB † 5.0V (Th : 0.7V)
16	SYNC-GND	GND for SYNC/HVCD block	
17	Cr1-IN	Input Y2/Cb1/Cr1 signal via clamp C	Y : 1 Vp-p(with sync) DC : 1.7V Cb/Cr : 0.7Vp-p(100% color bar) DC : 2.5V
18	Cb1-IN	nput Y2/Cb1/Cr1 signal via clamp C	Y: 1 Vp-p(with sync) DC: 1.7V Cb/Cr: 0.7Vp-p(100% color bar) DC: 2.5V
19	Y1-IN	nput Y2/Cb1/Cr1 signal via clamp C	Y: 1 Vp-p(with sync) DC: 1.7V Cb/Cr: 0.7Vp-p(100% color bar) DC: 2.5V
20	CLP-FIL	Connect Y-clamp filter	DC
21	Y-OUT	Output Y/Cb/Cr signal	DC Y:1.3V Cb/Cr:1.8V AC Y:0.7Vp-p (0 dB, non-sync) Cd/Cd.0.7Vp-p (0 dB)
22	Cb-OUT	Output Y/Cb/Cr signal	Pin to connect to the clock phase control resister
23	Cr-OUT	Output Y/Cb/Cr signal	System reset input pin . Pull-up resistor incorporaited. (Hysteresis input)
24	YS1(YCbCr2-in)	Selection SW for mainsignal and YCbCr2 input signal	1.0V † YCbCr2 † 5.0V (Th : 0.7V)

• Pin Function(2/2)

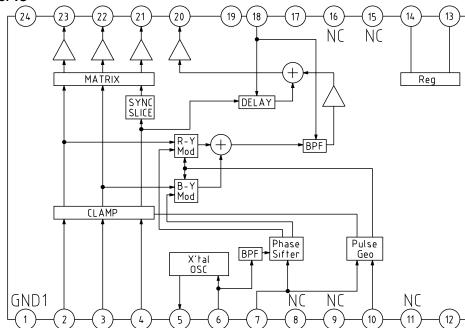
Pin No.	Pin Name	Function	IN/OUT SIGNAL
25	B1-IN	Input RGB1 signal via clamp C	0.7Vp-p DC : 2.5V
26	G1-IN	Input RGB1 signal via clamp C	0.7Vp-p DC: 2.5V
27	R1-IN	Input RGB1 signal via clamp C	0.7Vp-p DC : 2.5V
28	Y/C-GND	GND for Y/C/Text/Video-SW/1HDL	1.0V † YCbCr2 † 5.0V (Th: 0.7V)
29	Cr2-IN	Input Y2/Cb2/Cr2 signal via clamp C	Y: 1Vp-p (with sync) DC: 1.7V Cb/Cr: 0.7Vp-p (100% color bar) DC: 2.5V
30	Cb2-IN	Input Y2/Cb2/Cr2 signal via clamp C	Y: 1Vp-p (with sync) DC: 1.7V Cb/Cr: 0.7Vp-p (100% color bar) DC: 2.5V
31	Y2-IN	Input Y2/Cb2/Cr2 signal via clamp C	Y: 1Vp-p (with sync) DC: 1.7V Cb/Cr: 0.7Vp-p (100% color bar) DC: 2.5V
32	Y/C-Vcc	Vcc for Y/C/Text/Video-SW/1HDL	DC 5V
33	B2-IN	Input RGB2 signal via clamp C	0.7 : Vp-p DC : 2.5V
34	G2-IN	Input RGB2 signal via clamp C	0.7 : Vp-p DC : 2.5V
35	R2-IN	Input RGB2 signal via clamp C	0.7 : Vp-p DC : 2.5V
36	YS2/YM(RGB2-in)	Selection SW for main signal and RGB2 input signal	1.0V † YM † 1.5V 2.5V † RGB2 † 5.0V (Th1 : 0.7V, Th2 : 2.0V)
37	FIL	Connet : Y/C : Vcc	
38	XTAL	Connet 16.2 MHz Xtal	16.2 MHz wave
39	C3-IN	Input chroma signal via clamp C	0.3Vp-p DC : 1.6V
40	APC-FIL	Connect filter for chroma demodulation.	0.750
41	CVBS3/Y3-IN	Input CVBS3 or Y3 signal via clamp C	CVBS : 1Vp-p Y : 1Vp-p(with sync) DC : 1.8V
42	ADRESS	Set slave address.	88M/89H † 1.3V 3.9V † 8EH/8FH (Th1 : 1.5V, Th2 : 3.2V)
43	C2-IN	Input chroma signael via clamp C	0.3Vp-p (burst) DC : 1.6V
44	CVBS2/Y2-IN	Input CVBS2 or Y2 signal via clamp C	CVBS : 1Vp-p Y : 1Vp-p(with sync) DC : 1.8V
45	COMB SYS COLOR PLUG 46 M-PAL LOW LOW 4.43PAL SECAM High LOW 3.58/4.43 NTSC N-PAL High High	Output color system distinction result from this pin and Pin46	5V High OV Low
46	Fsc-OUT	Output sub carrier	AC: 0.84Vp-p DC: as shown in the figure below High (3.1V) (2.1V) Low
47	AFC-FIL	Connect filter for AFC detection	
48	C1-IN	Input chroma signal via clamp C	0.3Vp-p (burst) DC : 1.6V

DVR-7000

■ MM1394AF (SECAM ASSY : IC3601)

• NTSC/PAL Encoder IC

• Block Diagram

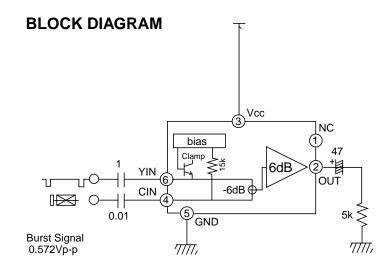


Pin Function

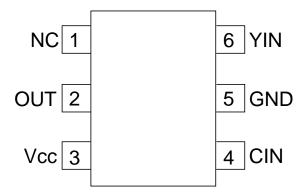
PIN No.	PIN NAME	FUNCTION
1	GND1	
2 3 4	R-Yin B-Yin Y+Sin	Input pins. Maximum input voltage: R-Y 1.00Vp-p B-Y 1.27Vp-p R-Y 1.00Vp-p (SYNC is 0.288Vp-p) DC level for clamp is 2.2V
5	X'tal out	Oscillator circuit output pin.
6	X'tal in	Subcarrier input pin.
7	NTSC/PAL	Mode setting pin NTSC: VCC PAL: PAL
8 9	NC	Open pin.
10	SYNCin	Composite sync signal input pin.
11	NC	Open pin.
12	Vcc1	
13	Iref	This pin sets internal reference current. Connect a 47k resistor between this pin and GND.
14	Vref	Internal reference voltage pin. Reference votage : 4V Connect a 10µF capacitor between this pin and GND.
15 16	NC	Open pin.
17	VIDEOout ON/OFF	This pin turns VIDEO output ON/OFF VIDEO output ON: GND VIDEO output OFF: VCC
18	f 0	This pin sets f0 for filter and delay circuits. NTSC: 20k PAL: 16k
19	Vcc2	Output stage power supply.
20	VIDEOout	Composite video signal output pin. This IC can drive 75 load.
21 22 23	Rout Gout Bout	RGB signal output pin.
24	GND2	Output stage GND.

■ MM1511XN (SCART ASSY : IC1401)

• Y/C Mix with Input Clamp

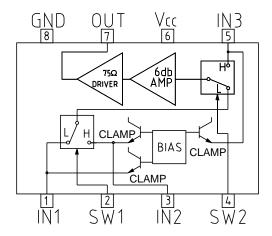


PIN CONFIGURATION



■ MM1228XF (SCART ASSY : IC1404)

- Video SW IC
 - Block Diagram



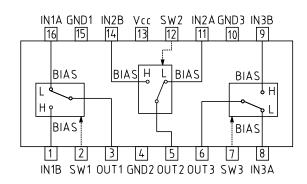
• Truth Table

Control Input Truth Table

SW1	SW2	OUT
L	L	IN1
Н	L	IN2
L/H	Н	IN3

■ MM1231XN (SCART ASSY : IC1406)

- Video SW IC
 - Block Diagram



• Truth Table

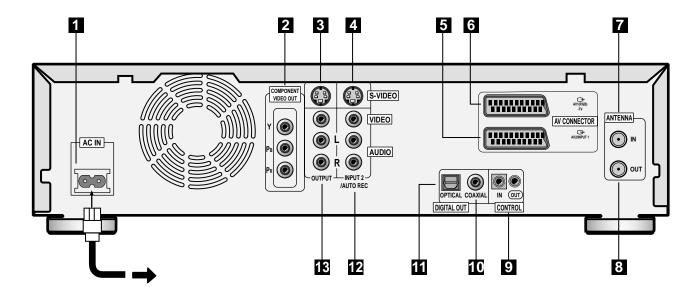
Control Input Truth Table

SW	SW	
L	IN1A	
	IN2A	
	IN3A	
R	IN1B	
	IN2B	
	IN3B	

7. PANEL FACILITIES AND SPECIFICATIONS 7.1 PANEL FACILITIES

■ REAR PANEL

WY and WV types



1 AC IN - Power inlet

2 COMPONENT VIDEO OUT

For connecting to a TV or monitor that has component video input

3 S-VIDEO OUTPUT

For connecting to a TV, monitor, AV receiver or other equipment with S-Video input

4 S-VIDEO INPUT

For recording from a camcorder, VCR or other equipment with S-Video output

5 AV2/INPUT 1 AV CONNECTOR

Audio/video input/output SCART-type connector for connecting to a VCR, or other equipment with a SCART connector. The video input/output is ordinary video or S-video only.

6 AV1(RGB)-TV AV CONNECTOR

Audio/video output SCART-type connector for connecting to a TV, or other equipment with a SCART connector. The video output is switchable between ordinary video ,S-video and RGB.

7 ANTENNA IN

Connect the TV antenna here.

8 ANTENNA OUT

Press the signal from the ANTENNA IN terminal to your TV.

9 CONTROL IN / OUT

Use for connecting to other Pioneer components bearing the Pioneer mark. Connect the CONTROL OUT of one component to the CONTROL IN of another using a mini-plug cord. The device at the beginning of the chain acts as the remote control sensor for everything in the chain.

10 DIGITAL OUT COAXIAL

For connecting to an AV receiver, Dolby Digital/ DTS/MPEG decoder or other equipment with coaxial digital input

11 DIGITAL OUT OPTICAL

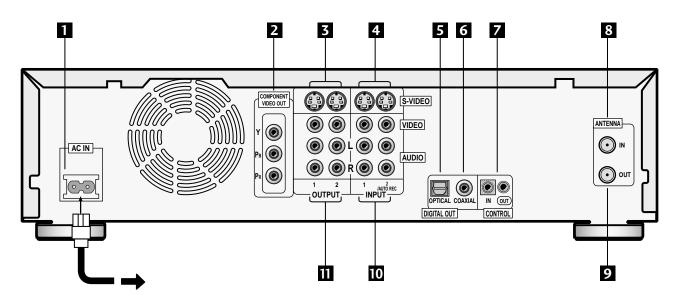
For connecting to an AV receiver, Dolby Digital/ DTS/MPEG decoder or other equipment with optical digital input

12 AUDIO/VIDEO input (INPUT 2/AUTO REC) For recording from a camcorder, VCR, satellite receiver or other equipment

13 AUDIO/VIDEO OUTPUT

For connecting to the audio and video inputs of a TV, monitor, AV receiver or other equipment

WL type



1 AC IN - Power inlet

2 COMPONENT VIDEO OUT

For connecting to a TV or monitor that has component video input

3 S-VIDEO OUTPUT 1, 2

For connecting to a TV, monitor, AV receiver or other equipment with S-Video input

4 S-VIDEO INPUT 1, 2

For recording from a camcorder, VCR or other equipment with S-Video output

5 DIGITAL OUT OPTICAL

For connecting to an AV receiver, Dolby Digital/ DTS/MPEG decoder or other equipment with optical digital input

6 DIGITAL OUT COAXIAL

For connecting to an AV receiver, Dolby Digital/ DTS/MPEG decoder or other equipment with coaxial digital input

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8 ANTENNA IN

Connect the TV antenna here.

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Press the signal from the ANTENNA IN terminal to your TV.

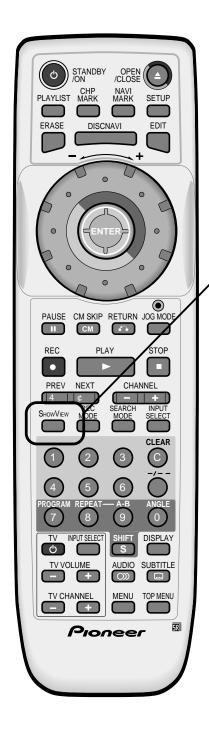
10 AUDIO/VIDEO INPUT 1, 2/AUTO REC

For recording from a camcorder, VCR, satellite receiver or other equipment

13 AUDIO/VIDEO OUTPUT 1, 2

For connecting to the audio and video inputs of a TV, monitor, AV receiver or other equipment

■ REMOTE CONTROL



ShowView (for WY type)

Press, then use the number buttons to enter a ShowView programming number for timer recording.

PlusCode (for WV type)

Press, then use the number buttons to enter a PlusCode programming number for timer recording.

G-code (for WL type)

Press, then use the number buttons to enter a G-code programming number for timer recording.

7.2 SPECIFICATIONS

Gene	ral	
Power r	equirements	deo, DVD-R/RW, Video-CD, CD
		60 W
		by mode 1.5 W (FL off)
		7.0 kg
		O (W) x 107 (H) x 373.5 (D) mm
Operatir	ng temperature	+5°C to +35°C
Operatir	ng numidity	5% to 85% (no condensation)
I V TOTTI	at	PAL/SECAM(tuner only)
Reco	rdina	
	•	DVD VideoRecording
Necolul	ng ionnat	DVD-VIDEC
Pacorda	able diece	DVD-ReRecordable
Nocorae	ibic discs	DVD-Recordable
Video r	ecording format	DVD Necordable
		13.5MHz
		MPEG
	ecording format	
		48kHz
		Dolby Digita
	ing time	
	V (VR mode)	
	,	Approx. 2 hours
	` '	Approx. 1–6 hours
	RW (Video mode)	, фр. ол
		Approx. 1 hour
		Approx. 2 hours
. =		
Tuner	•	

Receivable channels

Timer

Programs	1 month/8 programs
Clock	. Quartz lock (24-hour digital display)
Power off memory	Approx. 48 hours

Input/Output

input/Output
ANTENNA input/output terminal VHF/UHF set
75 Ω (coaxial)
Video input
Input level 1.0 Vp-p (75 Ω)
Jacks AV connector 2(Input 1), RCA jack(Input 2)
Video output
Output level
(for WY and WV types)
Jacks AV connector (Output 1), RCA jack(Output 2)
(for WL type)
Jacks RCA jack
S-Video input
Y (luminance) - Input level 1 Vp-p (75 Ω)
C (color) - Input level 300 mVp-p (75 Ω)
(for WY and WV types)
Jacks AV connector 2(Input 1), 4 pin mini DIN(Input 2,3)
(for WL type)
Jacks 4 pin mini DIN
S-Video output
Y (luminance) - Output level 1 Vp-p (75 Ω)
C (color) - Output level
(for WY and WV types)
Jacks AV connector 1(Output 1), 4 pin mini DIN(Output 2)
(for WL type)
Jacks 4 pin mini DIN
Component video output
Output levelΥ: 1.0 Vp-p (75 Ω)
$C_{\rm B}, C_{\rm R}$: 0.7 Vp-p (75 Ω)
Jacks RCA jacks
Audio input Input 1,2 (rear), 3 (front) L/R
Input level
During audio input
(Input impedence: more than $22k\Omega$)
(for WY and WV types)
Jacks AV Connector 2(Input 1), RCA jacks(Input 2,3)
(for WL type)
Jacks RCA jacks
Audio output Output 1,2 L/R
During audio output2V rms
(Output impedence: less than $1.5k\Omega$)
(for WY and WV types)
locks AV Connector 1/Output 1) BCA is also (Output 2)
Jacks AV Connector 1(Output 1),RCA jacks(Output 2)
(for WL type)
Jacks RCA jacks

	SECAN	И L ——	PAL B/G —		PALI	
	Frequency	Channel	Frequency	Channel	Frequency	Channel
VHF (low)	49 - 65 MHz	2 - 4	47 - 89 MHz	E2 - E4 X - Z	44 - 89 MHz	A - C X - Z
VHF (high)	104 - 300 MHz	5 - 10 B - Q	104 - 300 MHz	E5 - E12 S1 - S20 M1 - M10 U1 - U10	104 - 300 MHz	D - J 11, 13 S1 - S20
Hyper	300 - 470 MHz	S21 - S41	302 - 470 MHz	S21 - S41	302 - 470 MHz	S21 - S41
UHF	470 - 862 MHz	21 - 69	470 - 862 MHz	E21 - E69	470 - 862 MHz	E21 - E69

STEREO

B/G - A2

I - NICAM L - NICAM

B/G - NICAM

(for WY and WV types only)
AV Connectors(21-pin connector assignment)
AV connector input/output21-pin connector
This connector provides the video and audio signals for
connection to a compatible colour TV or monitor

PIN no.	
1	Audio 2/R out
2	Audio R in
11	G* out
3	Audio 1/L out
	R* or C* out or Cin
4	GND
6	Audio L in
17	GND
7	B* out or Cin
	Video out or Y* out
8	Status
20	Video in or Y in
21	GND
* AV CONNECTOR 4 (DOR)	TV/ 's sectional

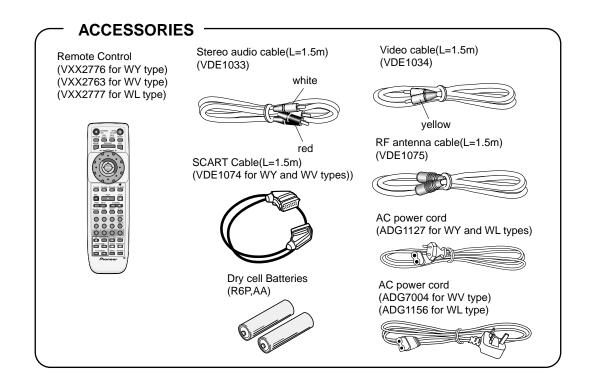
* AV CONNECTOR 1 (RGB)-TV is output.

(All types)

Control input/output Mini jack 1 each DV input/output 4 pin (i.LINK/IEEE 1394 standard)

Supplied accessories

Note: The specifications and design of this product are subject to change without notice, due to improvement.



Pioneer sound.vision.soul

Service Manual



ORDER NO. RRV2536

DVR RECORDER - 7000

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Туре	Model DVR-7000	Power Requirement	Region No.	Remarks
KU/CA	0	AC120V	1	
LB	0	AC110V	3	

 For R/RW Recorder section, this service manual includes only EXPLODEDE VIEWS except Traverce Mechanism Assy-s, Blockdiagram and MAIN ASSY contrast table. For the detail of R/RW Recorder section, refer to the service manual for DVR-A03 (Order No. RRV2423).

CONTENTS

Ί.	SAFETY INFORMATION	- 4
2.	EXPLODED VIEWS AND PARTS LIST	
3.	BLOCKDIAGRAM AND SCHEMATIC DIAGRAM \cdots	12
4.	PCB CONNECTION DIAGRAM	60
5.	PCB PARTS LIST	73
6.	ADJUSTMENT	8

7. GENERAL INFORMATION 8	35
7.1 DIAGNOSIS 8	35
7.1.1 MODEL TYPE AND REGION SETTING ··· 8	35
7.1.2 CPRM ID NUMBER AND ID DATA SETTING ··· 8	36
7.1.3 DEBUGGING MENU ······ 8	38
7.1.4 SERVICE MODE ······	94
7.1.5 POWER ON SEQUENCE	95
7.1.6 DISASSEMBLY ······	96
7.2 IC §	99
7.3 OUTLINE OF THE PRODUCT 15	50
8. PANEL FACILITIES AND SPECIFICATIONS ··· 15	57

1. SAFETY INFORMATION

This service manual is intended for qualified service technicians; it is not meant for the casual do-ityourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.

Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING

This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to cause cancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 - Proposition 65

NOTICE

(FOR CANADIAN MODEL ONLY)

Fuse symbols - (fast operating fuse) and/or - (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE

(POUR MODÈLE CANADIEN SEULEMENT)

Les symboles de fusible — (fusible de type rapide) et/ou — (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

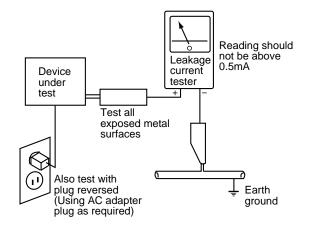
\cdot (FOR USA MODEL ONLY) $\, -$

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a Δ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

- IMPORTANT-

THIS PIONNER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

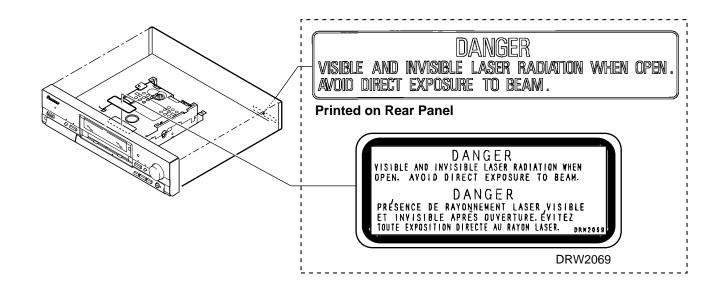
LASER DIODE CHARACTERISTICS – MAXIMUM OUTPUT POWER : 35 mw WAVELENGTH : 658 nm WARNING!

DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.



LASER
Picture 1
Warning sign for laser radiation

■ LABEL CHECK



Additional Laser Caution -

- The ON/OFF(ON:low level,OFF:high level) status of the CLAMP signals for detecting the loading state are detected by the drive CPUs, and the design prevents laser diode oscillation when the CLAMP signal turns OFF.
 - In normal operation, if no disc is clamped, the laser diode oscillation is disabled.
 - However, the interlock does not always operate in the test mode. $\ensuremath{^{*}}$
- When the cover is opened, close viewing of the objective lens with the naked eye will cause exposure to a Class 3A laser beam.

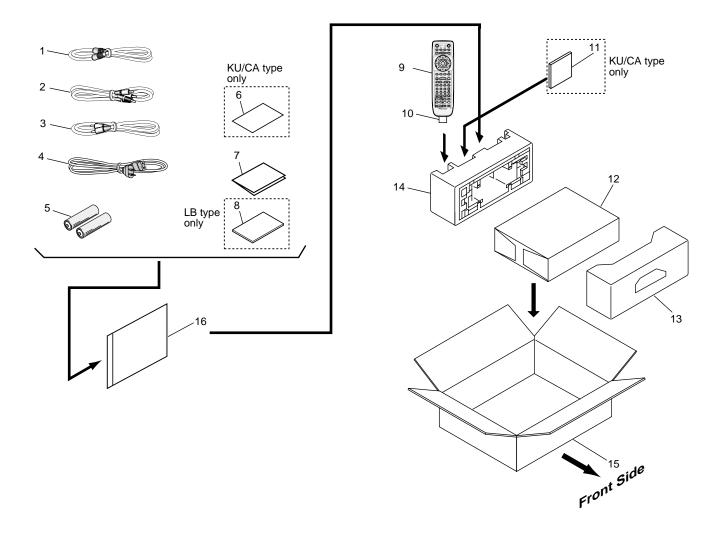
^{*} Refer to pages 43 of DVR-A03 Service Manual(RRV2423).

2. EXPLODED VIEWS AND PARTS LIST

NOTES: • Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.

- The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- Screws adjacent to ▼ mark on product are used for disassembly.

2.1 PACKING



(1)PACKING PARTS LIST

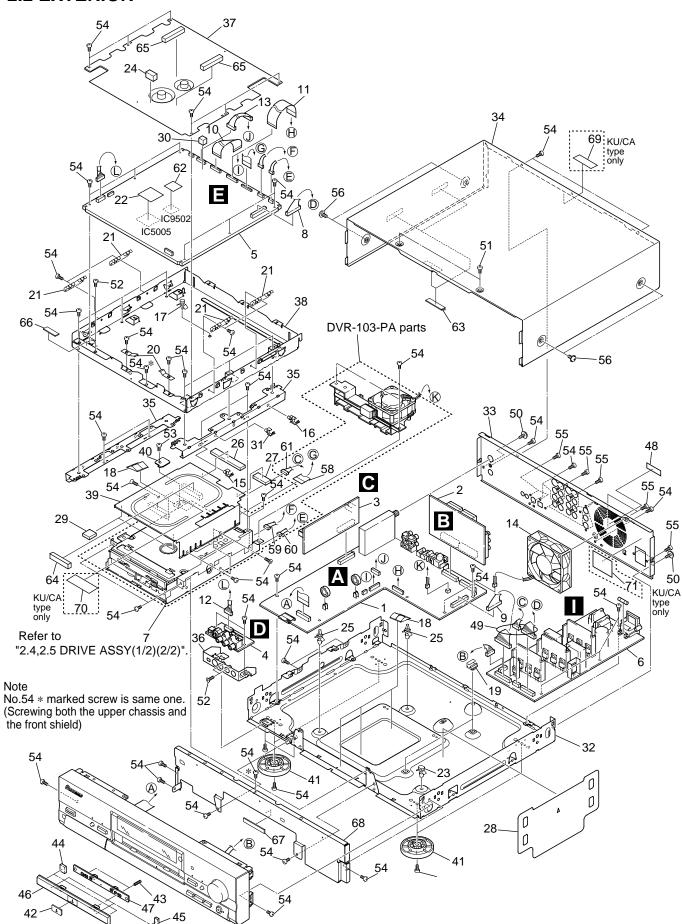
Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	RF Antenna Cable	VDE1025	NSP	11	DVD-RW Disc Ver.1.1	See Contrast table (2)
	2	Stereo Audio Cable	VDE1033		12	Mirror Sheet	VHL1006
	3	Video Cable	VDE1034		13	Front Pad (PS)	VHA1275
\triangle	4	AC Power Cord	ADG7021		14	Rear Pad (PS)	VHA1276
NSP	5	Battery (R6P,AA)	VEM-013		15	Packing Case	See Contrast table (2)
NSP	6	Warranty Card	See Contrast table (2)	NSP	16	Polyethylene Bag	Z21-038
	7	Operating Instructions	See Contrast table (2)			(230×340×0.03)	
	8	Operating Instructions	See Contrast table (2)				
	9	Remote Control Unit	See Contrast table (2)				
	10	Battery Cover	VNK4828				

(2) CONTRAST TABLE

DVR-7000/KU/CA and DVR-7000/LB are constructed the same except for the following:

Mark	No.	Cumbal and Deceription	Part	No.	Domonico
IVIAIN	140.	Symbol and Description	DVR-7000/KU/CA	DVR-7000/LB	Remarks
NSP	6	Warranty Card	ARY1026	Not used	
	7	Operating Instructions (English)	VRB1275	VRB1280	
	8	Operating Instructions (Chinese)	Not used	VRE1095	
	9	Remote Control Unit	VXX2763	VXX2777	
NSP	11	DVD-RW Disc Ver1.1	VZZ1001	Not used	
	15	Packing Case	VHG2122	VHG2152	

2.2 EXTERIOR



(1)EXTERIOR PARTS LIST

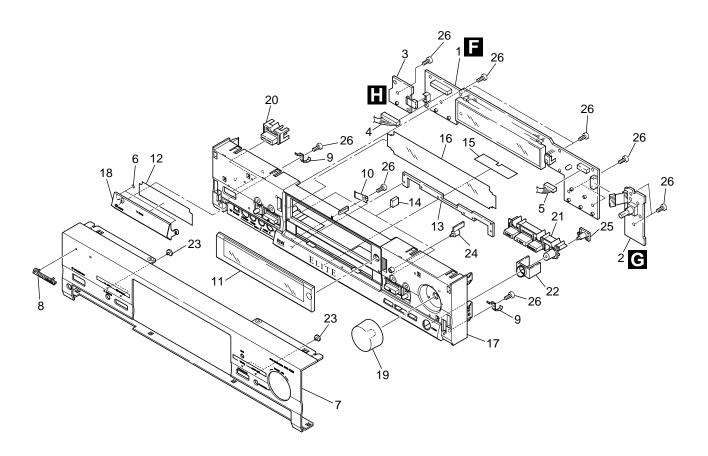
lark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	TUMJ ASSY	VWV1885	NSP	39	Shield Case(MTL)	VNE2260
	2	REAR JACK ASSY	VWV1887	NSP	40	Plate(MTL)	VNE2265
	3	3D Y/C ASSY	VWV1888		41	Insulator(ABS)	VXA2424
	4	FRONT JACK ASSY	VWV1886		42	DVD Badge(PC)	VAM1119
	5	MAIN ASSY	VWV1894		43	Tray Spring(BK)	VBH1337
A		DOWED OURDLY 4 00Y	\			T 0	\/E00000
\triangle	6 7	POWER SUPPLY ASSY DVD-R/RW UNIT	VWR1347 DVR-103-PA		44 45	Tray Spacer Tray Cushion S	VEC2239 VEC2263
						-	
	8	Connector Assy	PF14PP2S30		46	Tray Panel(ABS)	VNK4801
		(MAIN ASSY CN2003 ↔POWER ASSY CN201)	1	NSP	47 48	Tray Holder(ABS) ID Label	VNK4809 VRW1877
	9	Connector Assy	PF16PP2S30	NOF	40	ID Label	VIXVVIOII
	Ū	(TUMJ ASSY CN2001			49	Binder	PEC-107
		⇔POWER ASSY CN202)					
	10	Flexible Cable(20P)	VDA1875		50	Screw(Steel)	ABA7008
		(TUMJ ASSY CN2010			51	Screw(Steel)	VBA1082
		↔MAIN ASSY CN2001)			52	HLS Screw(Steel)	ABA7029
		,			53	Screw	BBZ26P050FMC
	11	Flexible Cable(22P)	VDA1876				
		(TUMJ ASSY CN1003			54	Screw	BBZ30P060FMC
		→MAIN ASSY CN7001)			55	Screw	BPZ30P080FZK
	12	Housing Assy(6P)	VKP2263		56	Screw	FBT40P080FNI
		(FRONT-J ASSY CN2004			57	• • • • • •	
		→MAIN ASSY CN9001)			58	FFC Cable(40P)	DDD1192
	13	Housing Assy(10P)	VKP2264			(MAIN ASSY CN3001↔	
		(TUMJ ASSY CN3001 →MAIN ASSY CN8001)				RECORDER DRIVE MAIN CN409	9)
	14	DC FAN Motor	VXM1092		59	Housing Assy(6P)	DKP3550
ISP	15	Locking Wire Saddle	DEC1305		39	(MAIN ASSY CN6001↔	DKF 3330
		3					7)
ISP	16	Wire Saddle	DEC1450		00	RECORDER DRIVE MAIN CN407	,
	17	Card Spacer	DEC1772		60	Housing Assy(4P)	DKP3551
	18	Stick Finger	DNB1092			(MAIN ASSY CN2002↔	
ISP	19	P.Plate Holder	PNY-405			RECORDER DRIVE MAIN CN406	,
.0.	20	Earth Plate(Cu)	VBK1070		61	Connector Assy	PF06PP2S42
	20	Latti Flate(Ou)	VBICTOTO			(POWER ASSY CN203↔	
	21	Earth Metal(Cu)	VBK1094		00	RECORDER DRIVE MAIN CN403	,
	22	Cooling Sheet (23×23)	VEB1332		62	Coolig Sheet S	VEB1333
	23	Card Spacer	VEC1708		63	Gasket	VEC2235
	24	Spacer	VEC2157				
	25	Locking Card Spacer	VEC2234		64	Gasket(L)	VEC2252
	25	Locking Card Spacer	VLO2234		65	Gasket(M)	VEC2253
	26	Duot Spager A	VEC2237		66	Gasket(T)	VEC2267
	26	Dust Spacer A			67	Gasket(N)	VEC2273
	27	Dust Spacer B	VEC2238		68	Front Shield(MTL)	VNE2261
	28	Barrier Sheet(PPE)	VEC2251			,	
	29	Dust Spacer C	VEC2261		69	65 Label	See Contrast table (2)
	30	Spacer	VEC2262		70	Fuse Caution Label	See Contrast table (2)
					71	Fuse Caution Label	See Contrast table (2)
ISP	31	Wire Saddle(5S)	VEC2270			. 400 044.10.1. 2420.	(2)
ISP	32	Chassis(FE)	VNA2277				
	33	Rear Panel(FE)	See Contrast table (2)				
	34	Bonnet(FE)	VXX2814				
ISP	35	Upper Frame(FE)	VNE2244				
ISP	36	Input Plate	VNE2245				
ISP	37	Upper Plate Assy	VNE2272				
ISP	38	Upper Chassis(MTL)	VNE2259				
ISP	37	Upper Plate Assy	L)	VNE2272	VNE2272	VNE2272	VNE2272

(2) CONTRAST TABLE

DVR-7000/KU/CA and DVR-7000/LB are constructed the same except for the following:

Mark	No.	O Symbol and Description	Part	No.	Domosko
	110.	Symbol and Description	DVR-7000/KU/CA	DVR-7000/LB	Remarks
	33	Rear Panel	VNA2328	VNA2329	
	69	65 Label	ARW7050	Not used	
	70	Fuse Caution Label	VRW1902	Not used	
	71	Fuse Caution Label	VRW1903	Not used	

2.3 FRONT PANEL



(1)FRONT PANEL PARTS LIST

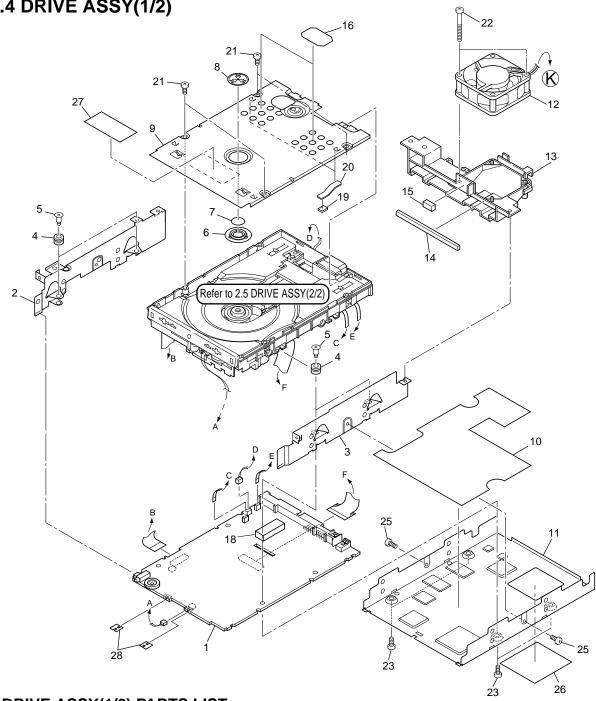
Mark	No.	Description	Part No.
	1	FLASSY	VWG2314
	2	JOG ASSY	VWG2316
	3	SW ASSY	VWG2315
	4	Flexible Cable(20P)	VDA1874
		(FL ASSY CN1202↔	
	_	TUMJ ASSY CN2009)	
	5	Connector Assy	PF07PP2S17
		(FL ASSY CN1201↔ POWER ASSY CN204)	
		FOWER ASST CIN204	1
	6	Cushion Rubber	AEB7068
	7	Front Aluminium(AL)	See Contrast table (2)
	8	Pioneer Badge(AL)	VAM1124
	9	Earth Plate(Cu)	VBK1133
	10	Door Spring(SUS)	VBK1134
	11	FL Window(PMMA)	VEC2197
	12	Input Sheet(PC)	VEC2199
	13	Drive Sheet(EPDM)	VEC2275
	14	Drive Cushion	VEC2258
	15	Drive Filter	VEC2259
	16	FL Filter(PC)	VEC2260
	17	Panel Base(ABS)	See Contrast table (2)
	18	Input Door(ABS)	See Contrast table (2)
	19	Dial Knob(ABS)	VNK4802
	20	Power Button(ABS)	VNK4803
	21	Play Button(ABS)	VNK4804
	22	Record Ring(ABS)	VNK4805
	23	Combined Lens(MMA/BS)	VNK4806
	24	DVD Lens(MMA/BS)	VNK4807
	25	Record Lens(MMA/BS)	VNK4827
	26	Screw	BPZ30P080FZK

(2) CONTRAST TABLE

DVR-7000/KU/CA and DVR-7000/LB are constructed the same except for the following:

Mark	No.	Symbol and Description	Part	No.	Remarks
IVIAIN	140.	Symbol and Description	DVR-7000/KU/CA	DVR-7000/LB	Remarks
	7 17 18	Front Aluminium(AL) Panel Base(ABS) Input Door(ABS)	VAH1392 VNK4983 VNK4924	VAH1378 VNK4799 VNK4800	

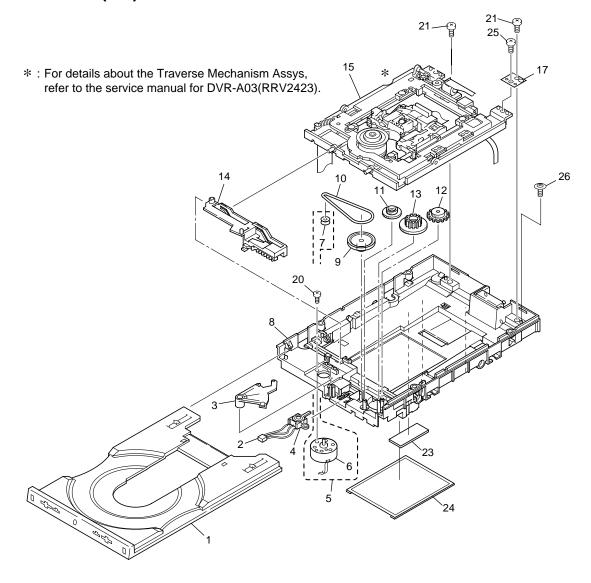
2.4 DRIVE ASSY(1/2)



● DRIVE ASSY(1/2) PARTS LIST

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	RECORDER DRIVE MAIN	DWX2148		15	Duct Seal B	VEC2209
NSP	2	Flame L	VNE2242	NSP	16	Dust Sheet	VEC2236
NSP	3	Flame R	VNE2243		17	•••••	
	4	Float Rubber	DEB1466		18	Air Cushion	DEB1488
	5	Float Screw	DBA1148		19	Spacer POR	DEB1483
	6	Clamper	DNK3829		20	Plate	DNK3839
	7	Clamper Yoke	DNH2467		21	Screw	BPZ26P060FZK
	8	Upper Clamper	DNK3830		22	Screw	BPZ30P350FZK
	9	Clamper Holder	DNC1548		23	Screw	PMA26P060FMC
	10	Radiate Sheet	DEB1473		24	•••••	
	11	Base Chassis	DNC1549		25	Screw	DBA1159
	12	DC Fan Motor	AXM7014		26	Label	DRW2053
NSP	13	Fan Duct	VNK4796		27	Caution Label	DRW2069
	14	Duct seal A	VEC2208		28	Acetate Tape	DEH1021

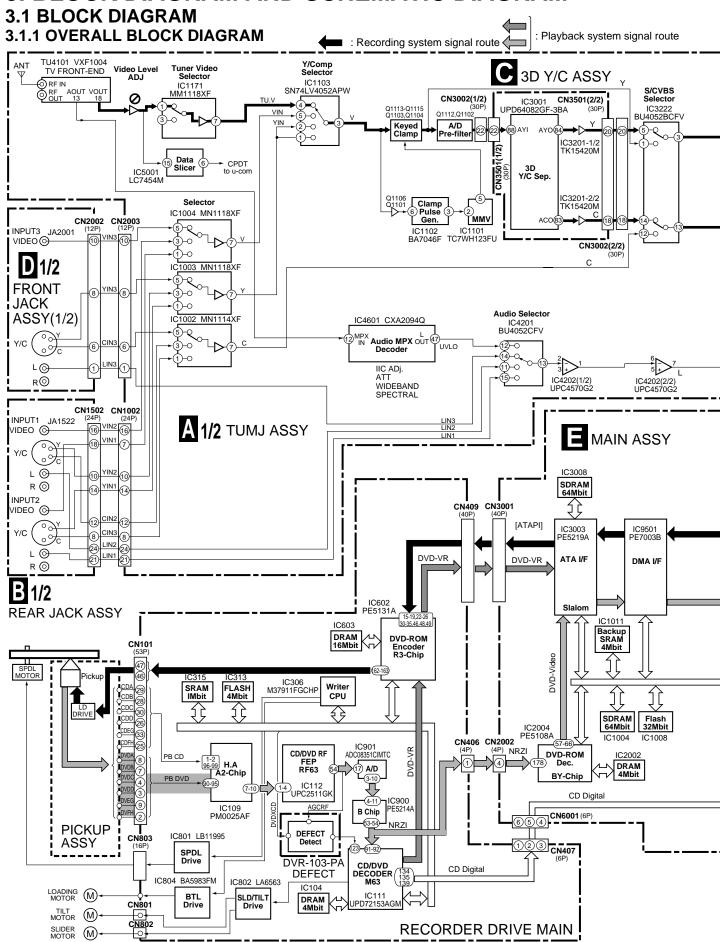
2.5 DRIVE ASSY(2/2)

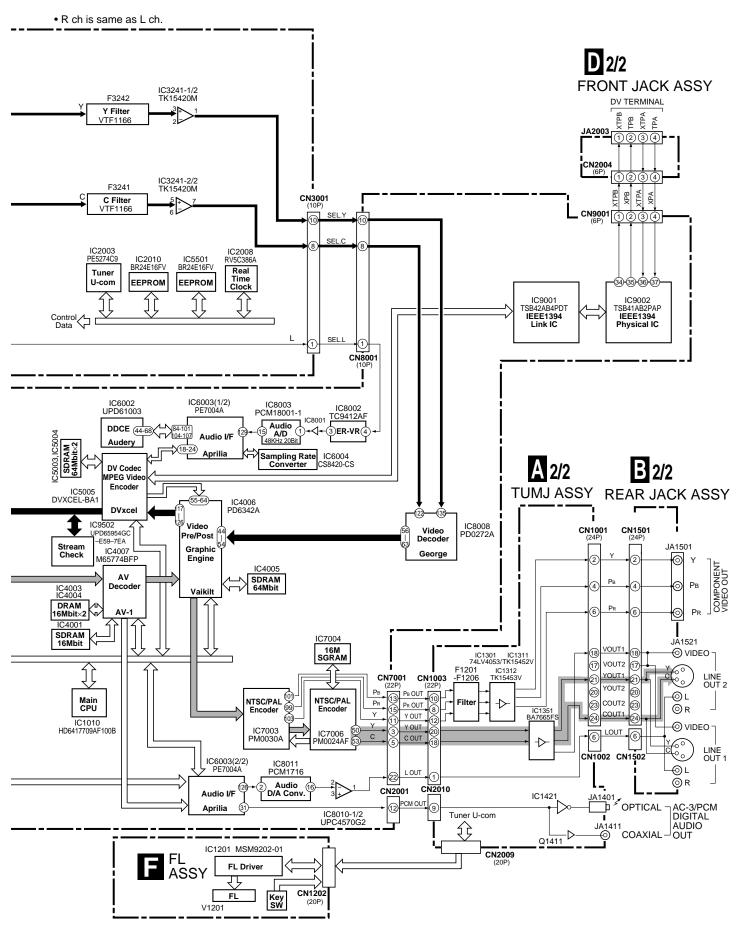


● DRIVE ASSY(2/2) PARTS LIST

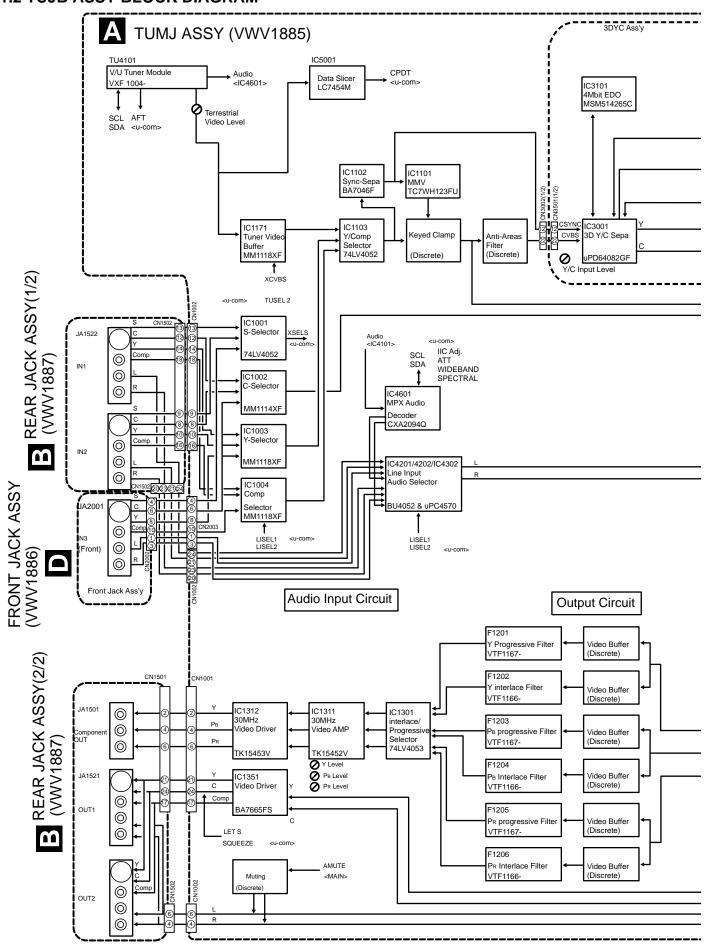
Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	Tray	VNK4808		16	•••••	
	2	Connector Assy(3P)	DKP3544		17	Plate	DBK1208
	3	Eject Lever	DNK3817		18	•••••	
	4	Lever Switch	DSK1001		19	•••••	
	5	Loading Motor Assy-s	DXX2491		20	Screw	JGZ17P030FMC
NSP	6	Carriage Motor	RXM1090		21	Screw	BPZ26P060FZK
	7	Motor Pulley	PNW1634		22	•••••	
NSP	8	Loading Base	DNK3811		23	Air Cushion	DEB1488
	9	Gear Pulley	DNK3813		24	Sheet (Rubber)	DEC2411
	10	Belt (Rubber)	DEB1465		25	Screw	BMZ26P050FMC
	11	Gear A	DNK3814		26	Screw	VBA1034
	12	Gear C	DNK3816				
	13	Gear B	DNK3815				
NSP	14	Clamp Cam	DNK3818				
NSP	15	Traverse Mechanism Assy-s	DXB1744				

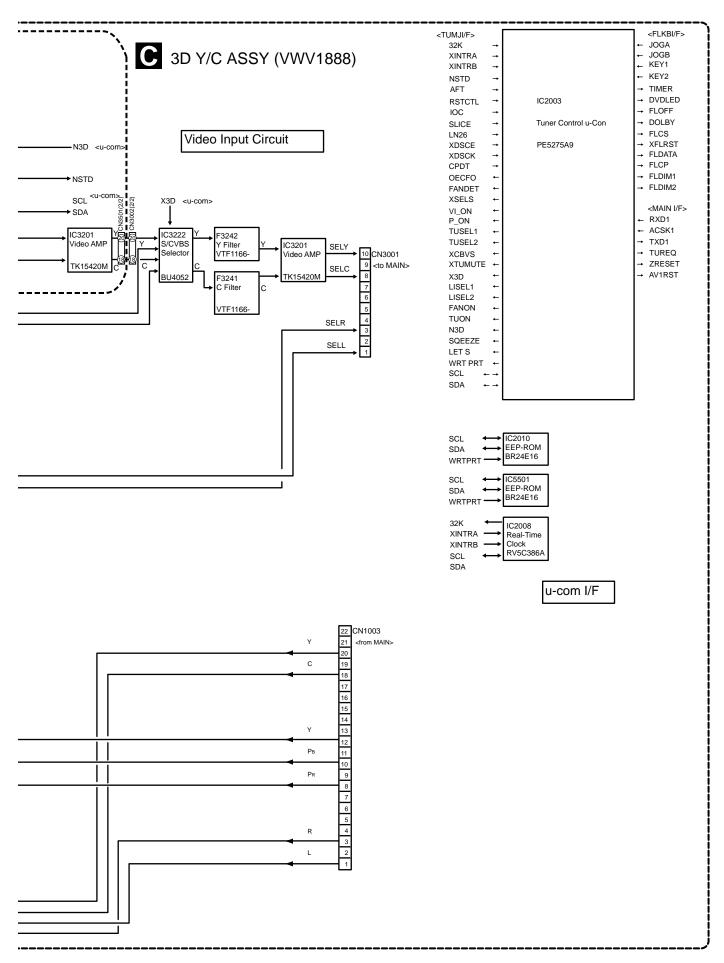
3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM



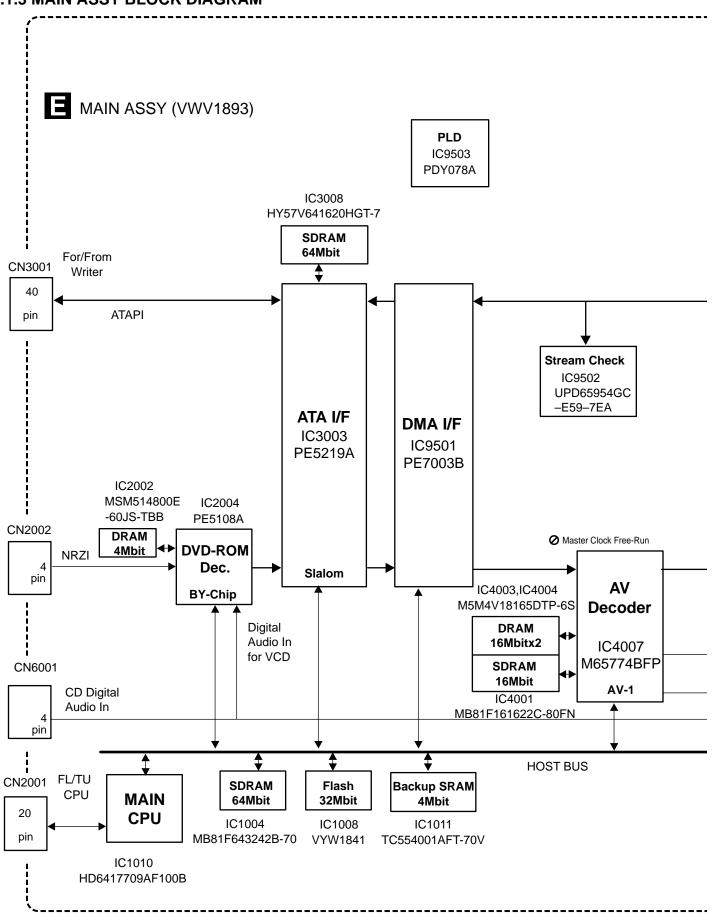


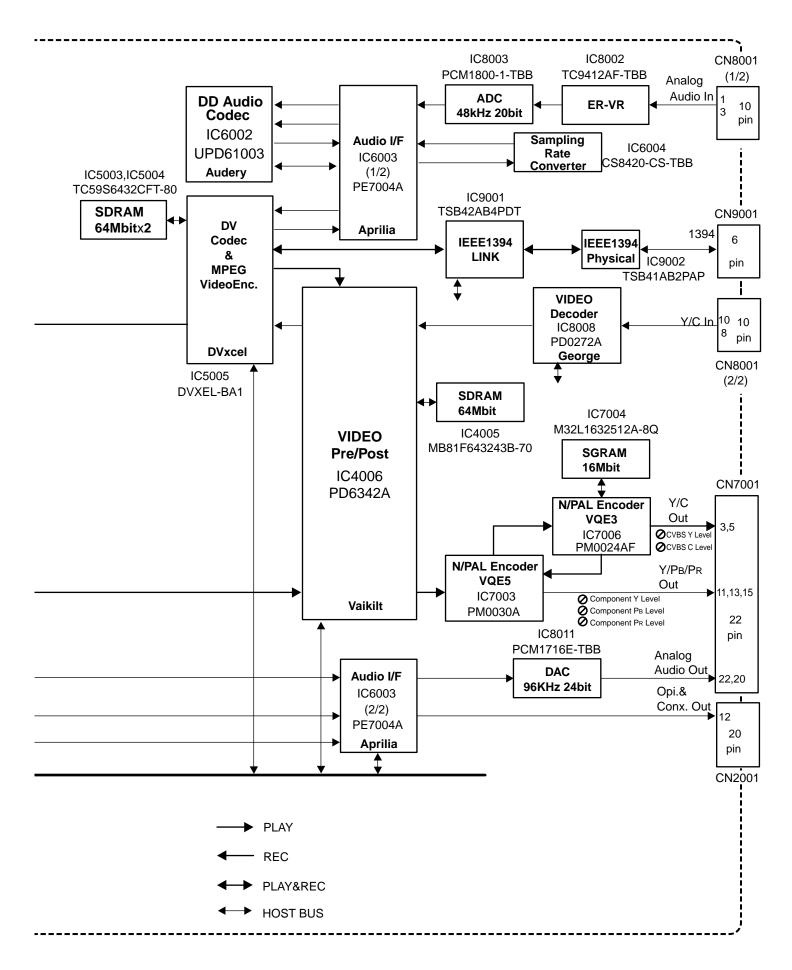
3.1.2 TUJB ASSY BLOCK DIAGRAM



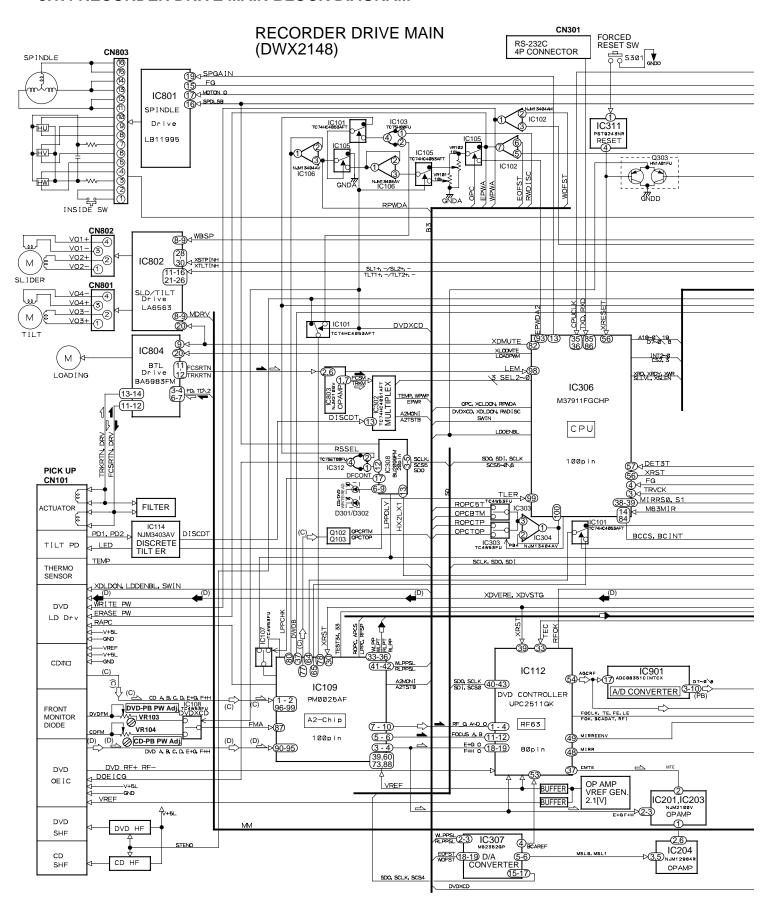


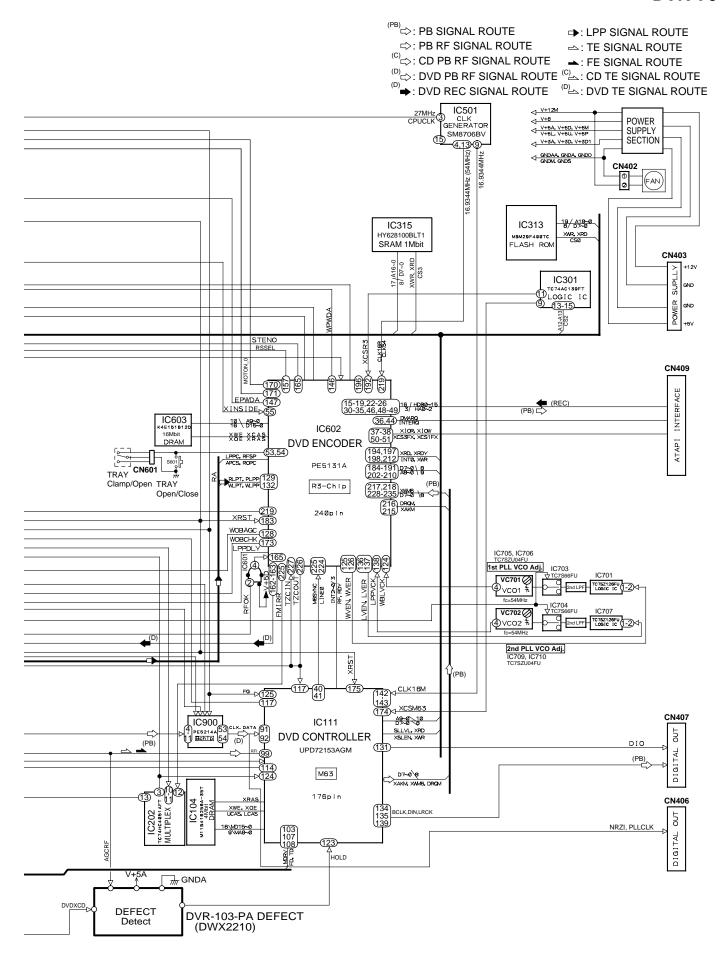
3.1.3 MAIN ASSY BLOCK DIAGRAM



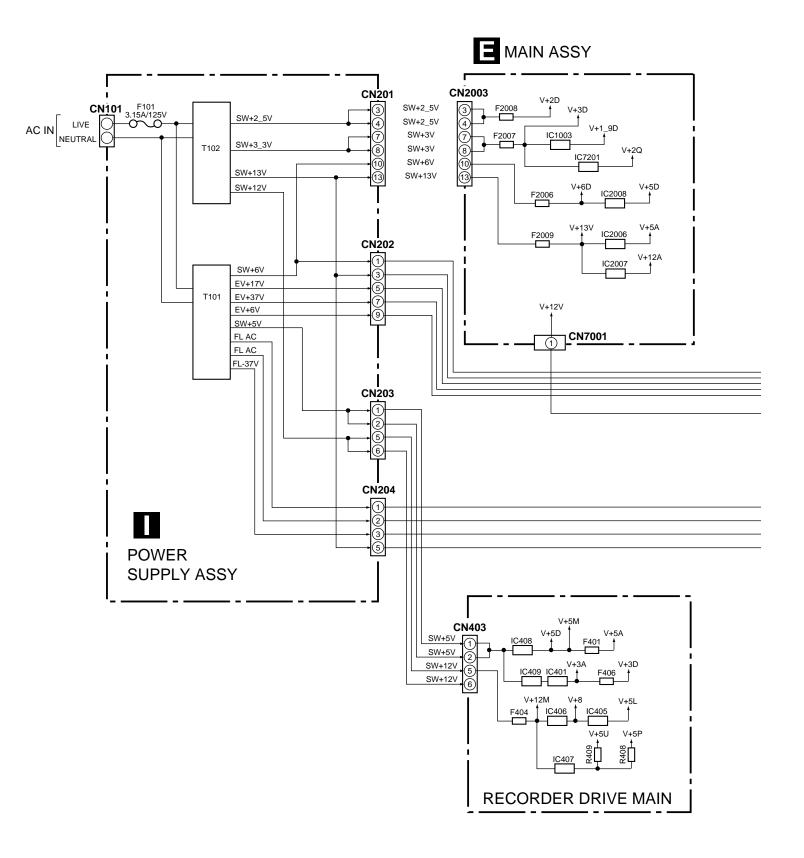


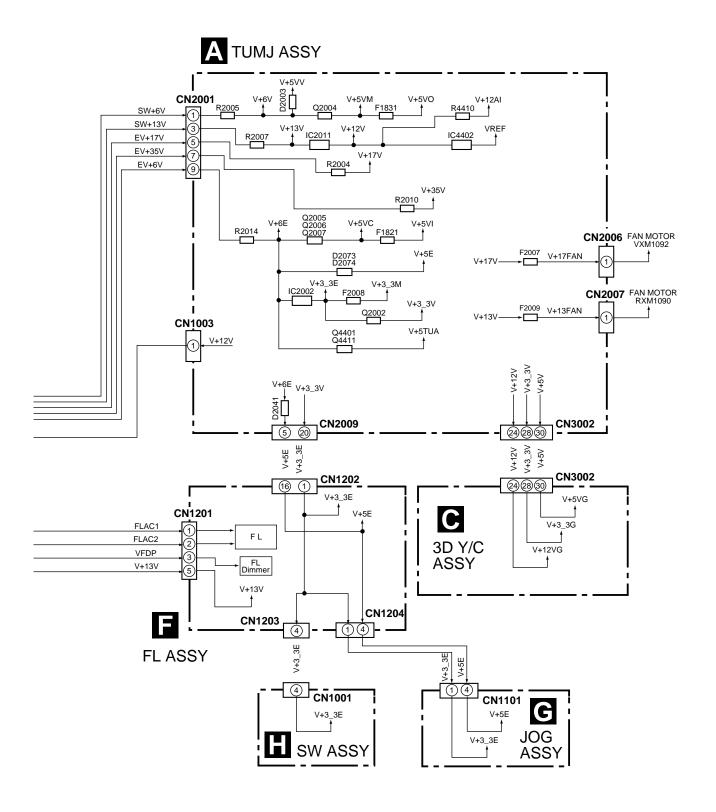
3.1.4 RECORDER DRIVE MAIN BLOCK DIAGRAM



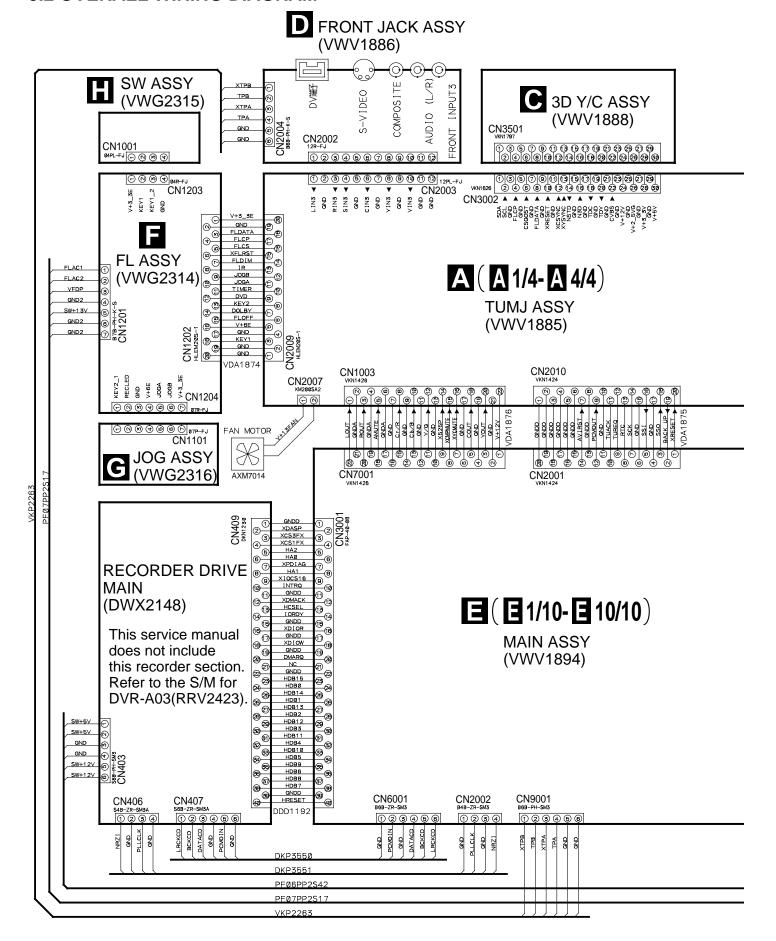


3.1.5 POWER BLOCK DIAGRAM

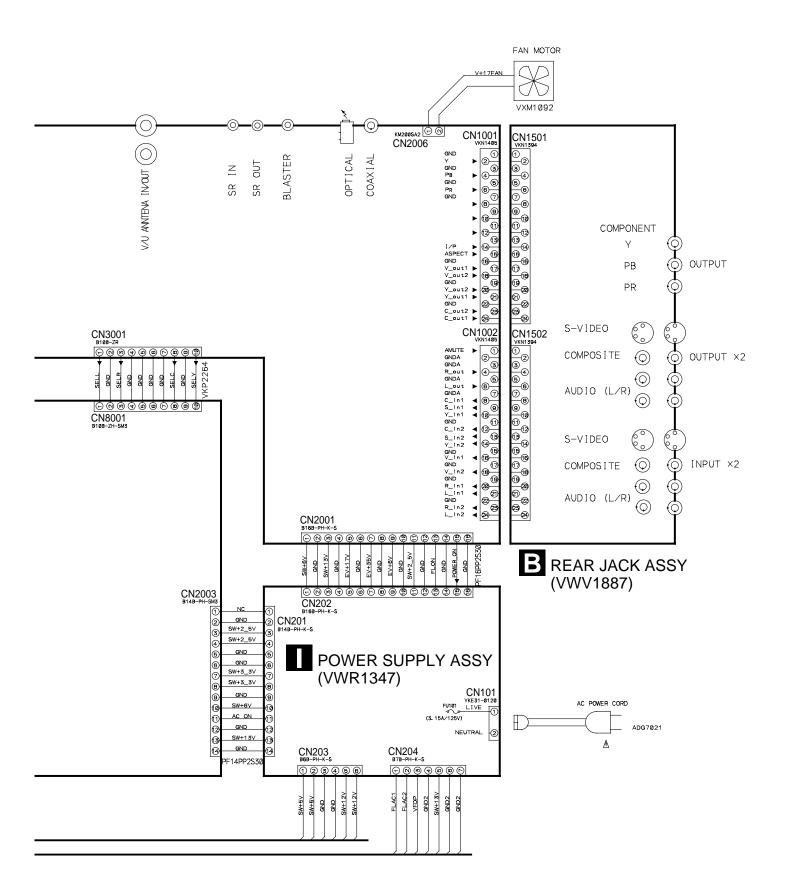




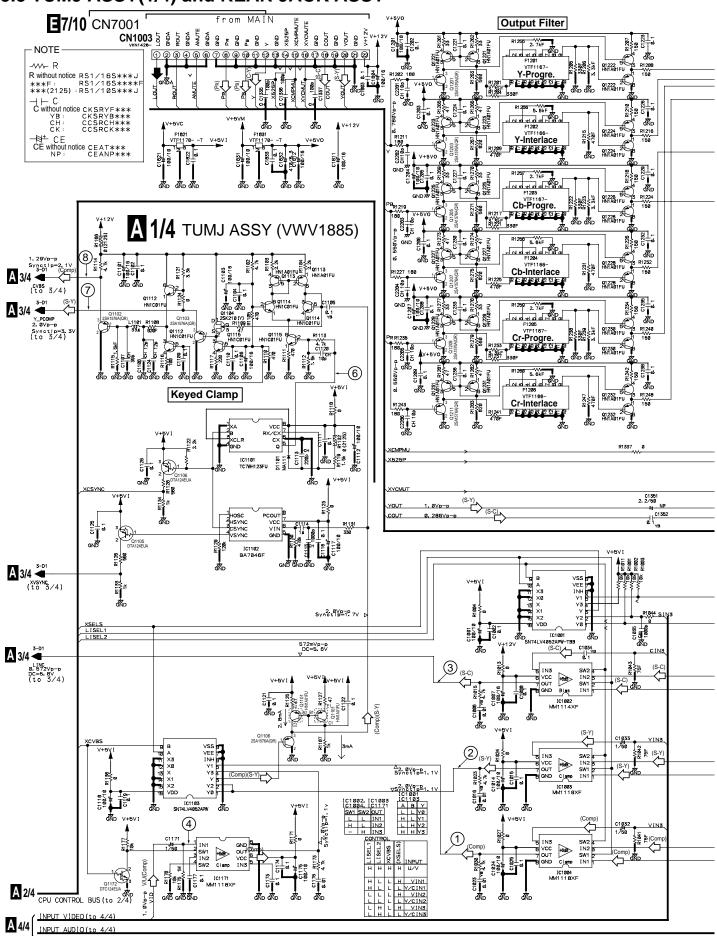
3.2 OVERALL WIRING DIAGRAM



Note: When ordering service parts, be sure to refer to "EXPLODED VIEWS and PARTS LIST" or "PCB PARTS LIST".



3.3 TUMJ ASSY(1/4) and REAR JACK ASSY

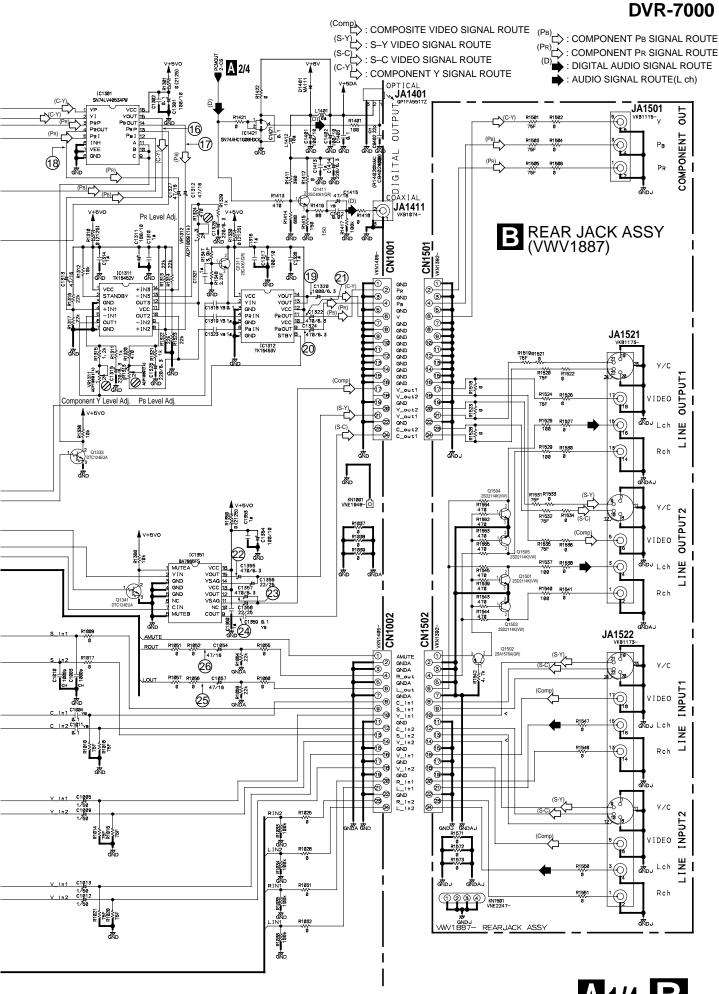


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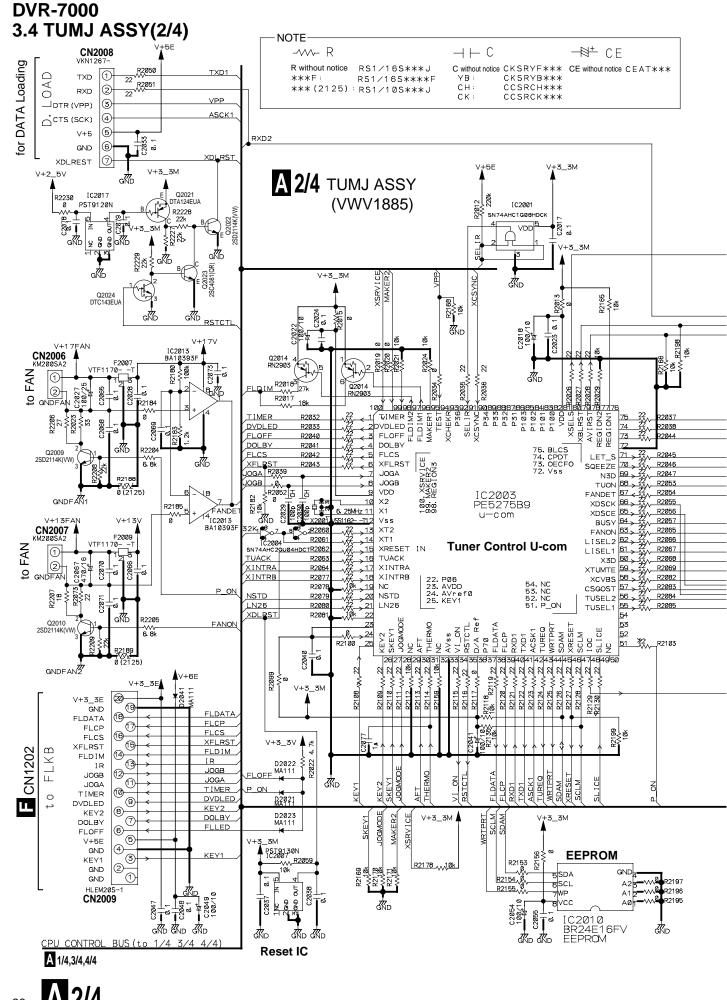


A 1/4 B

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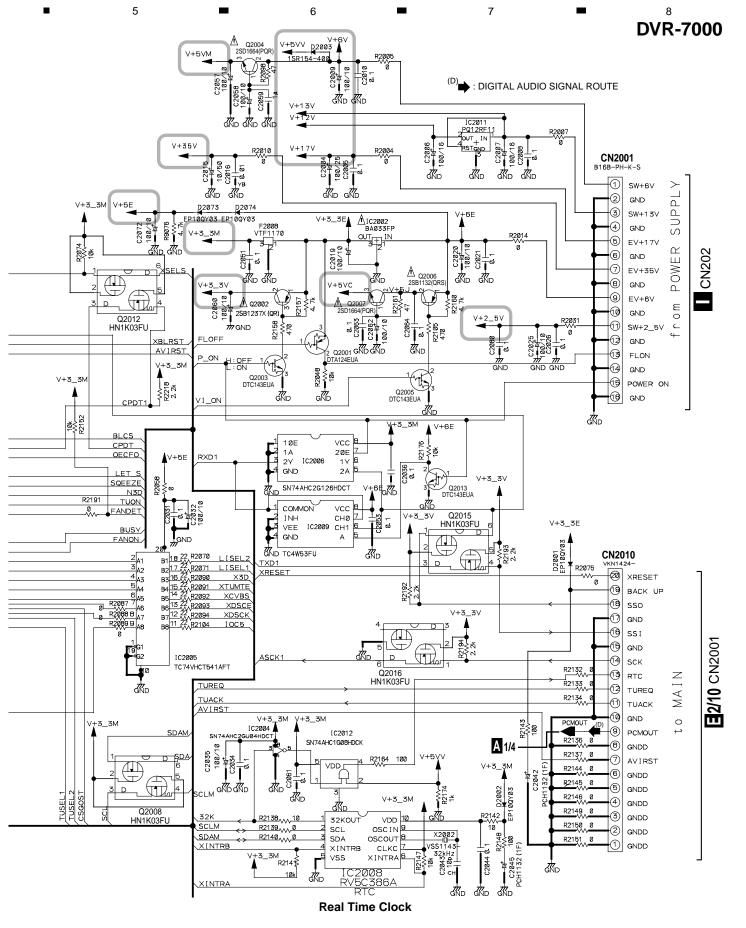
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В



: The power supply is shown with the marked box.

A 2/4 27

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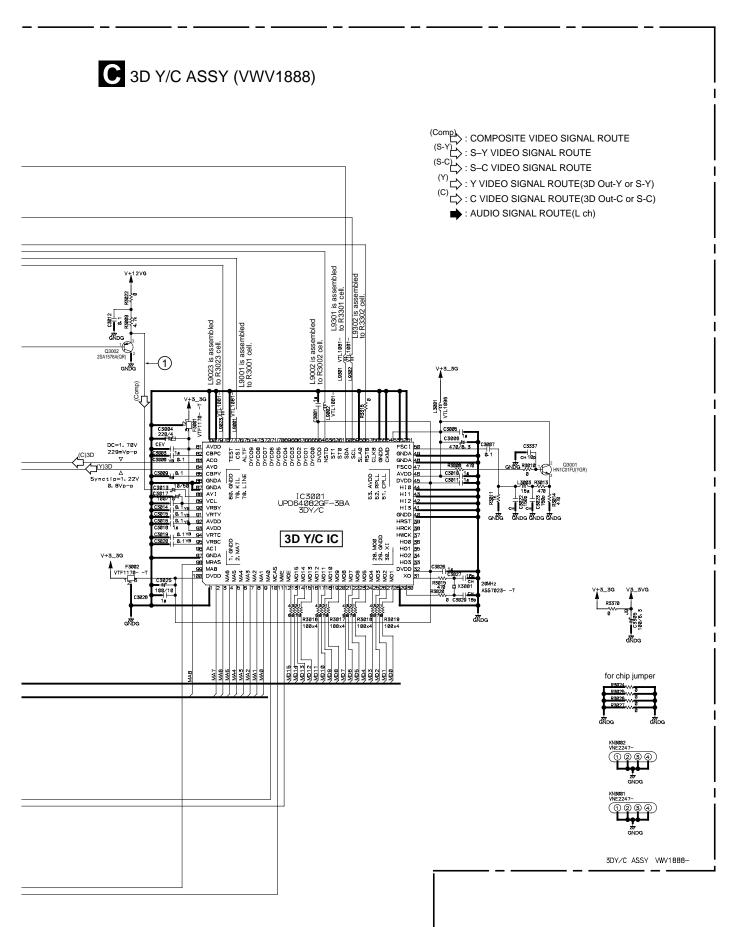
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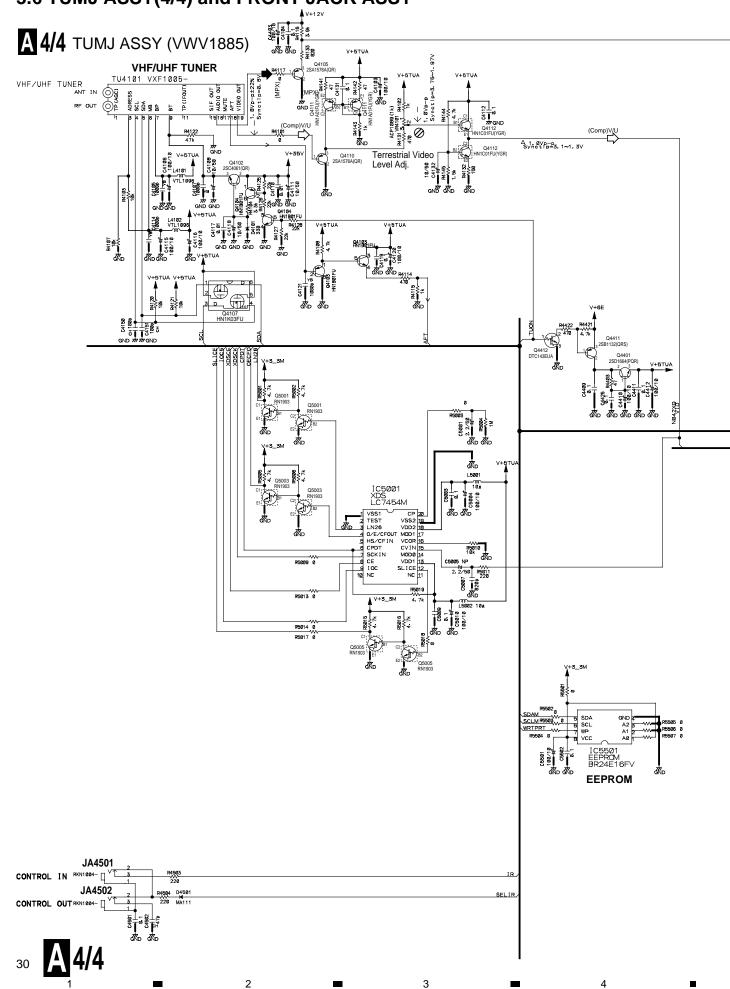
A 3/4 C 29

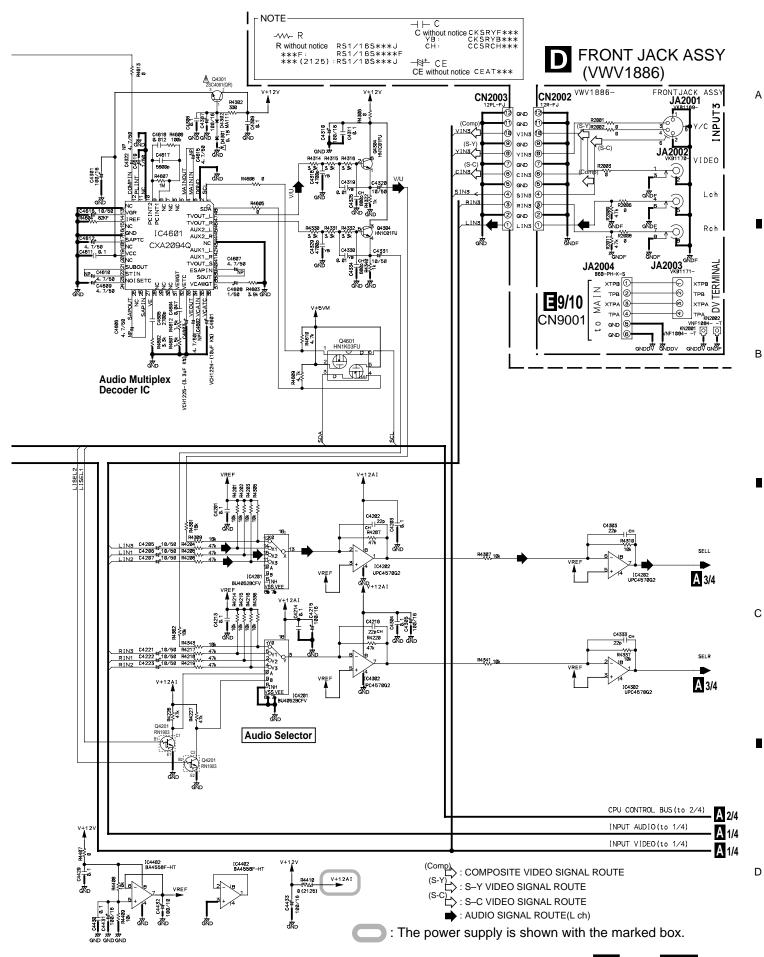
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D

3.6 TUMJ ASSY(4/4) and FRONT JACK ASSY





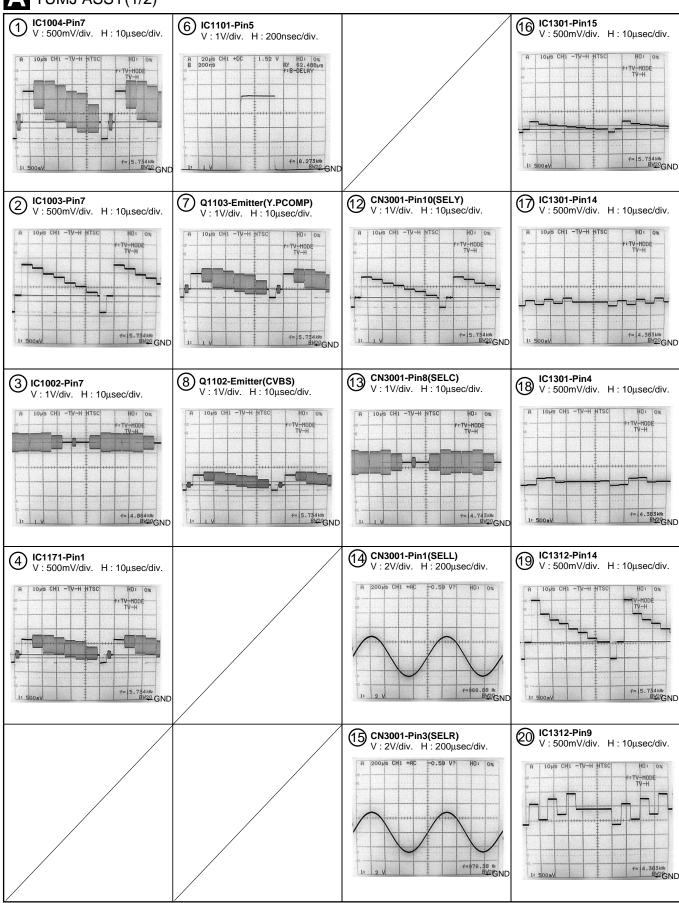
A 4/4 D

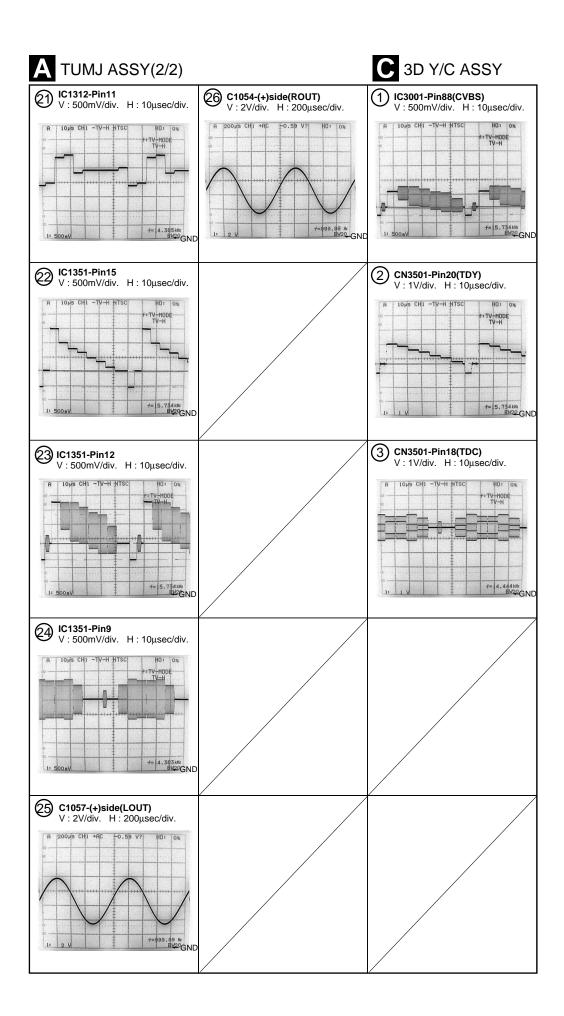
■ WAVEFORMS

Note: The encircled numbers denote measuring point in the schematic diagram.



TUMJ ASSY(1/2)

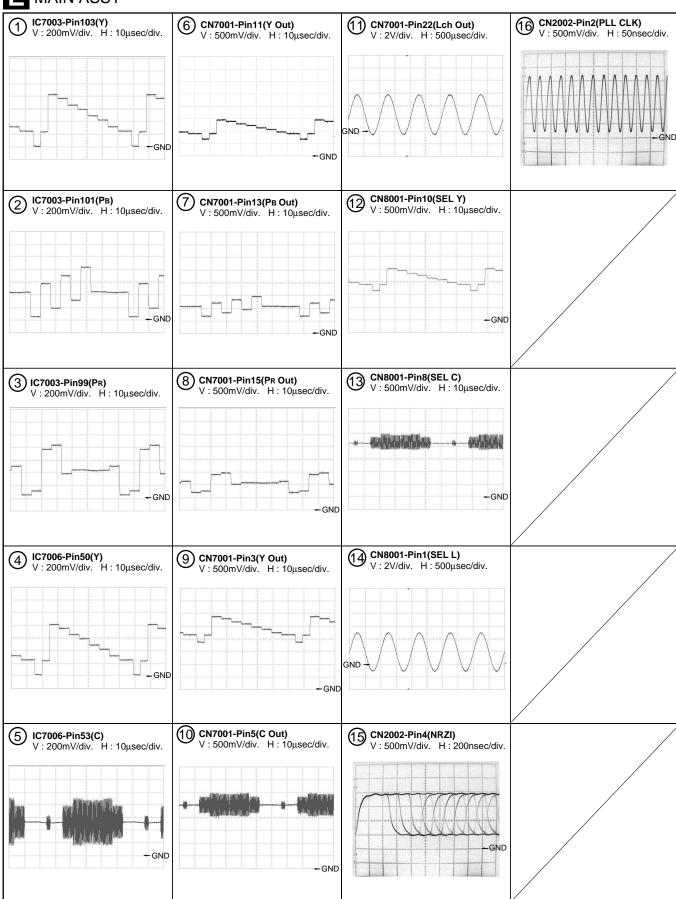


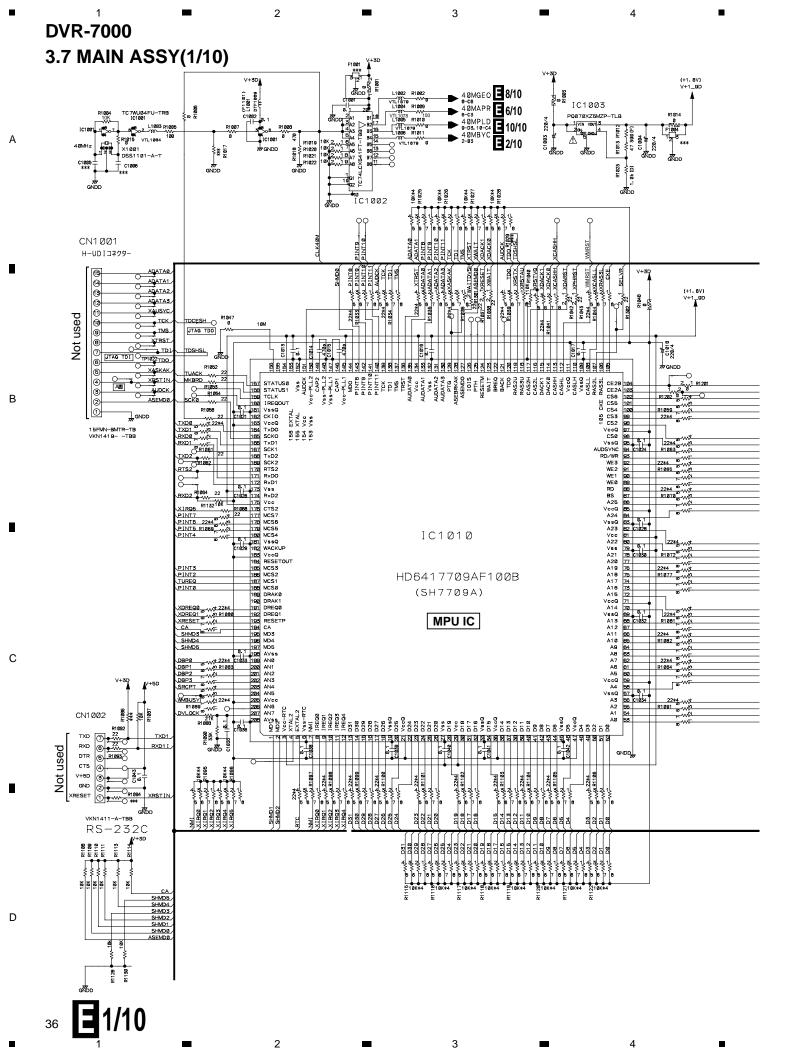


■ WAVEFORMS

Note: The encircled numbers denote measuring point in the schematic diagram.

MAIN ASSY





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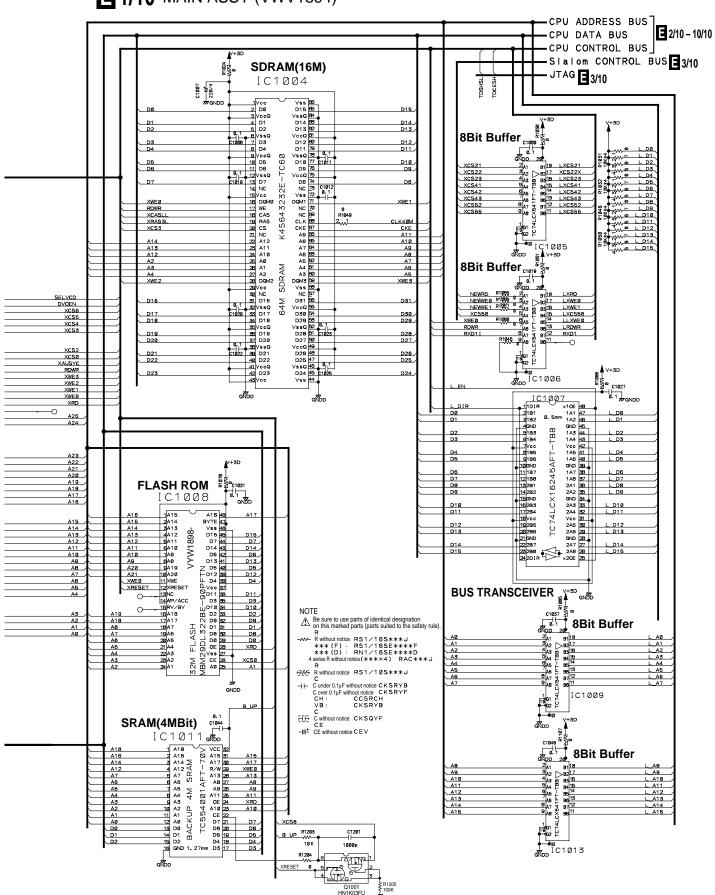
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1/10 MAIN ASSY (VWV1894)

6

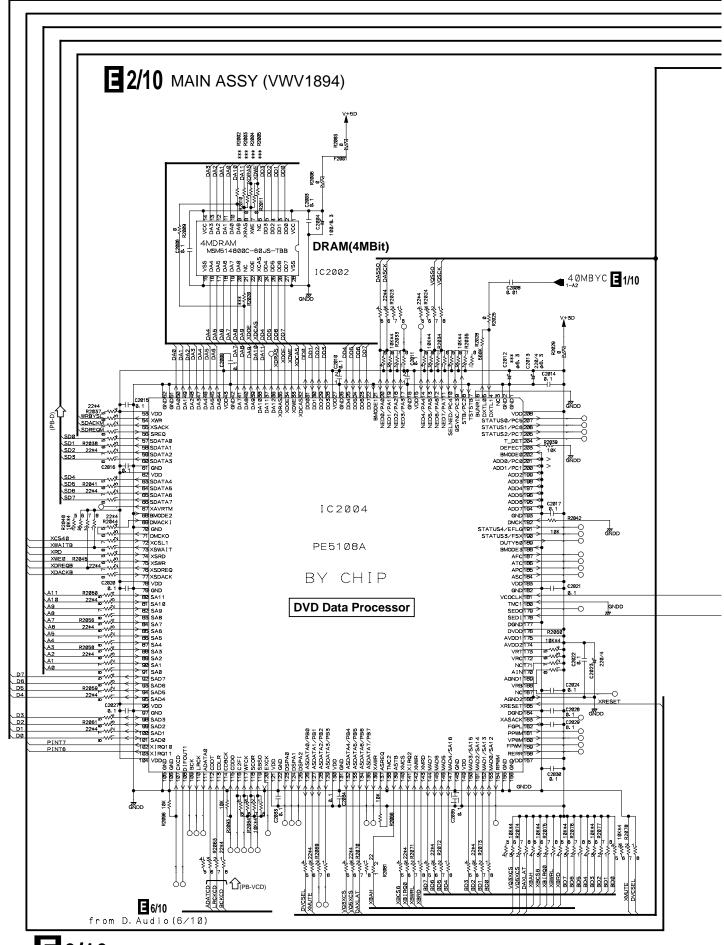
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1/10 37

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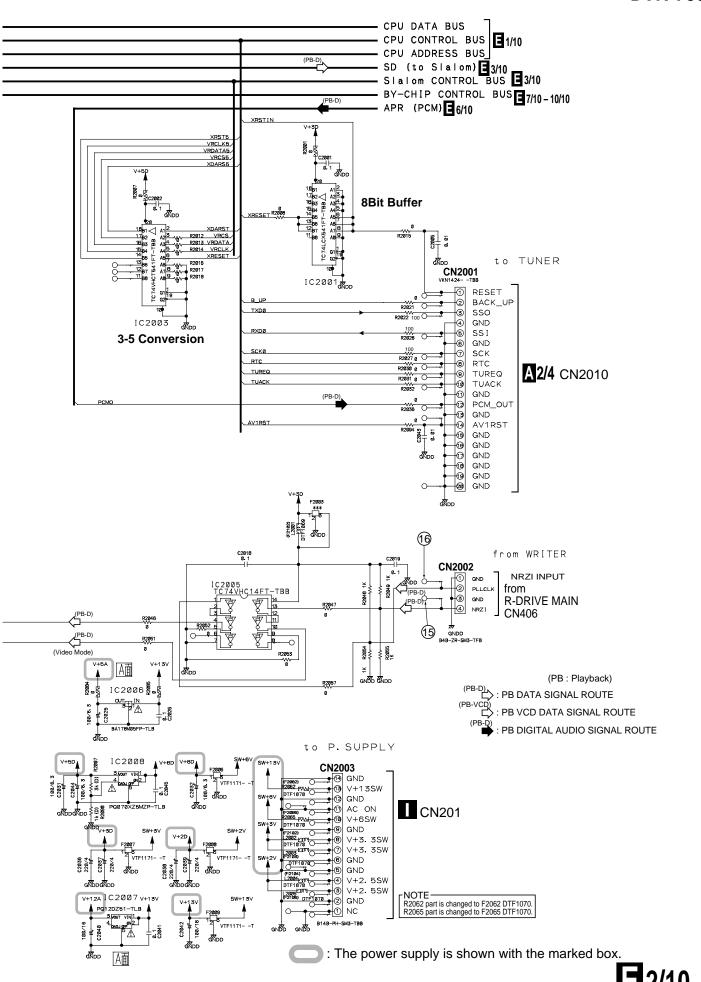
D

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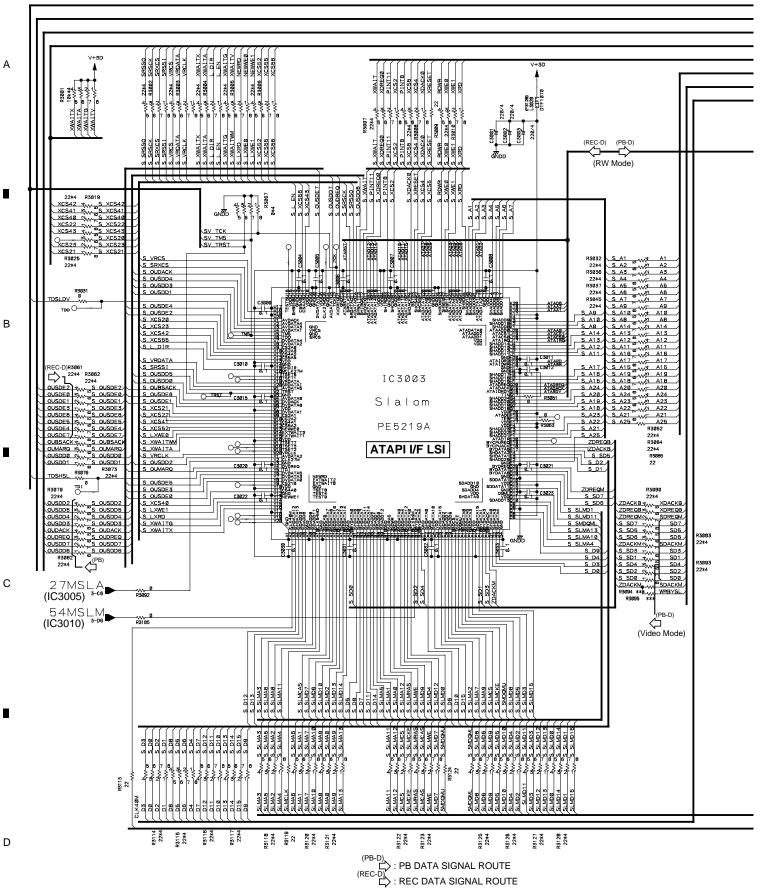
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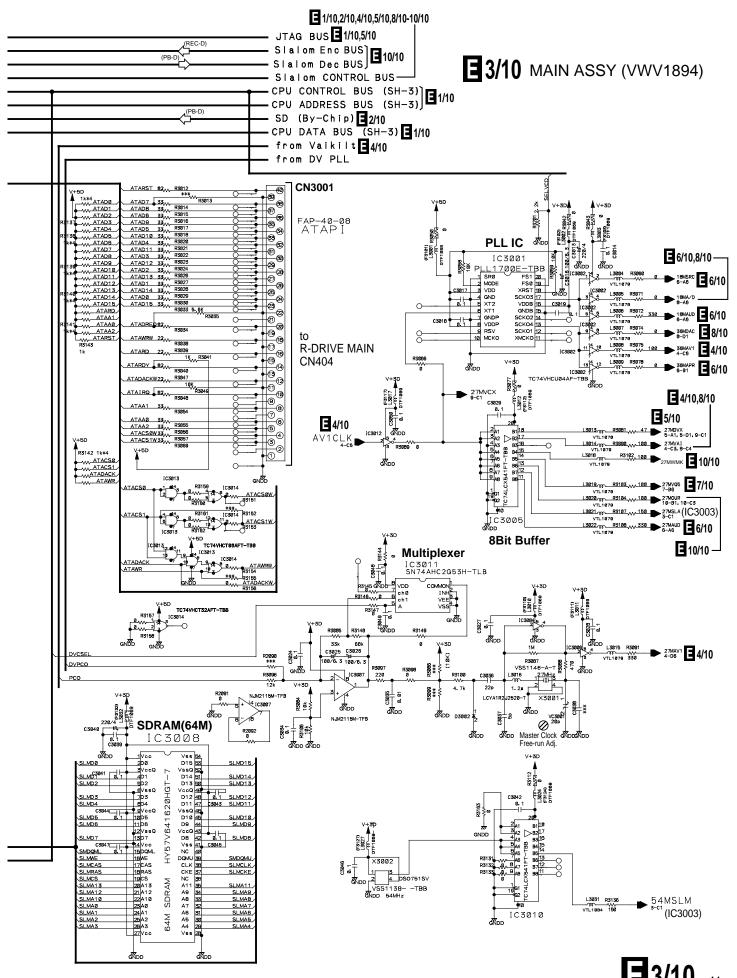
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2/10 3



40 **3/10**



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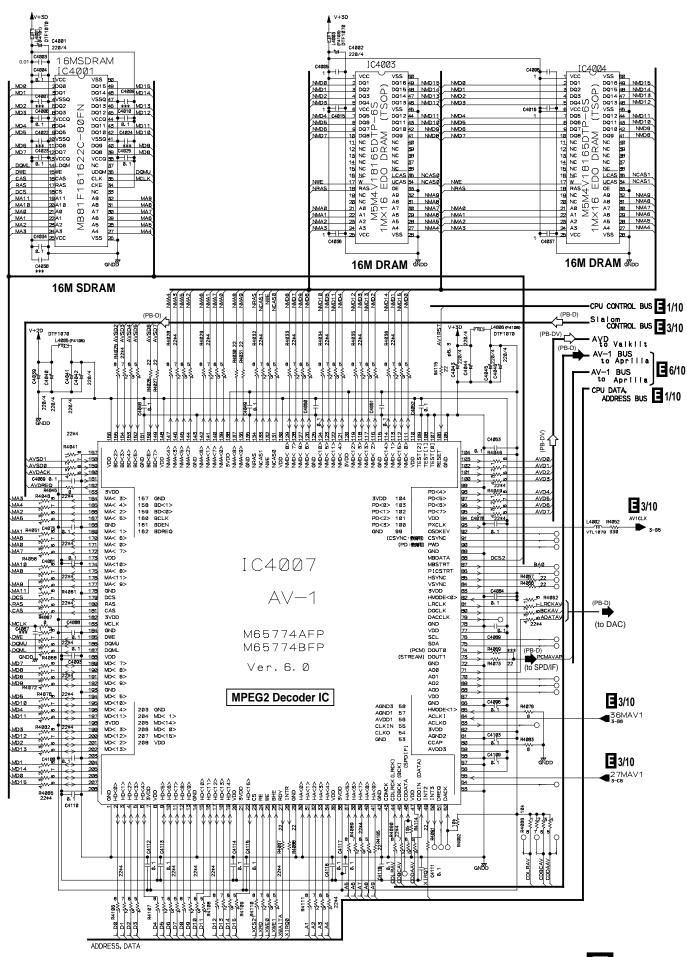
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4/10 43

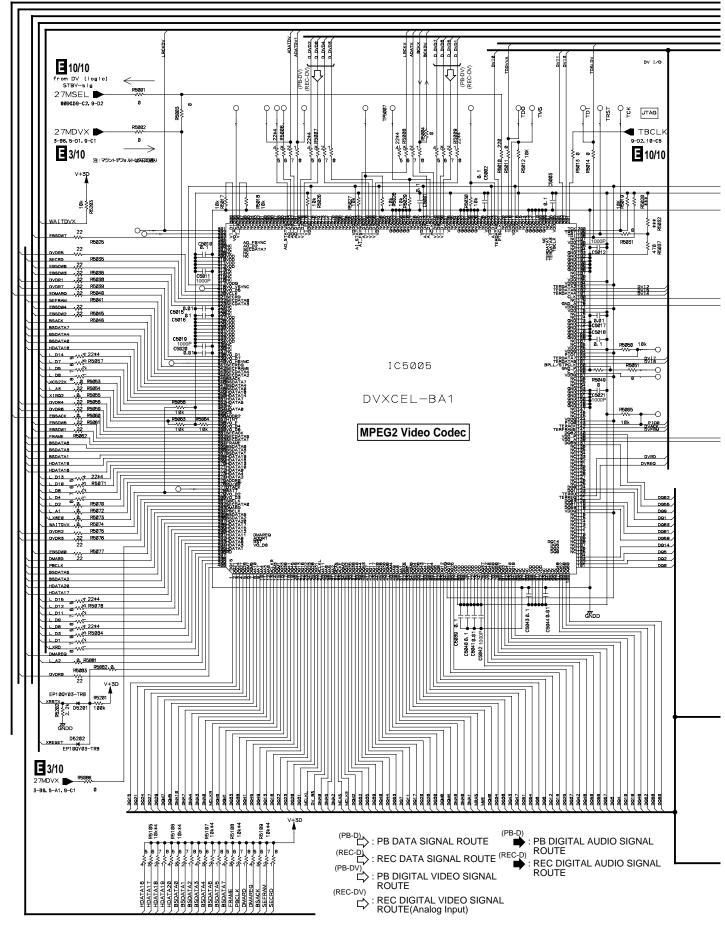
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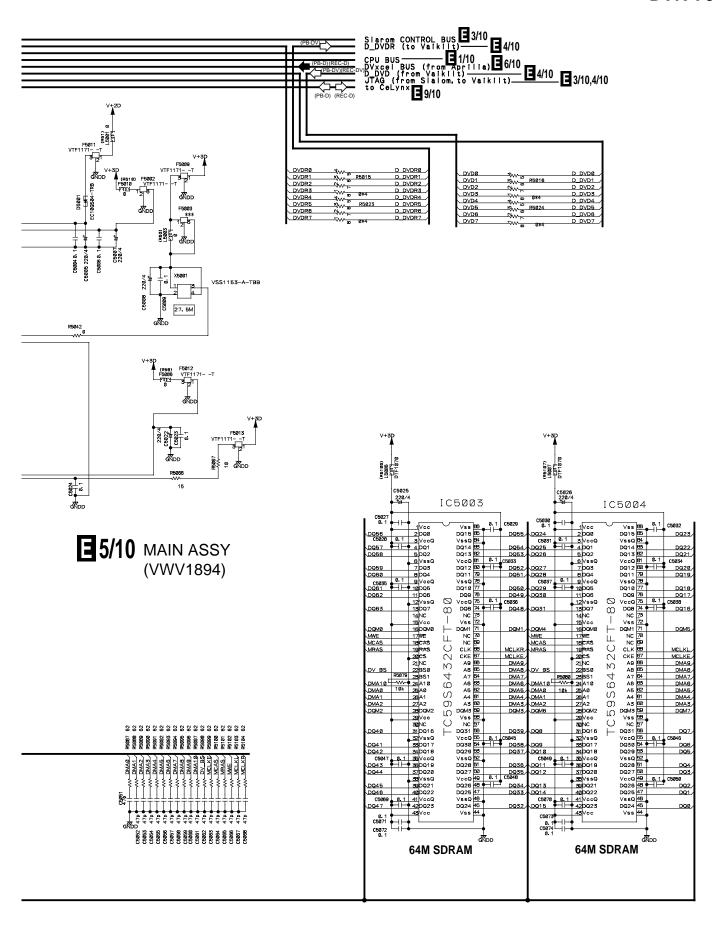
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44 3 5/10

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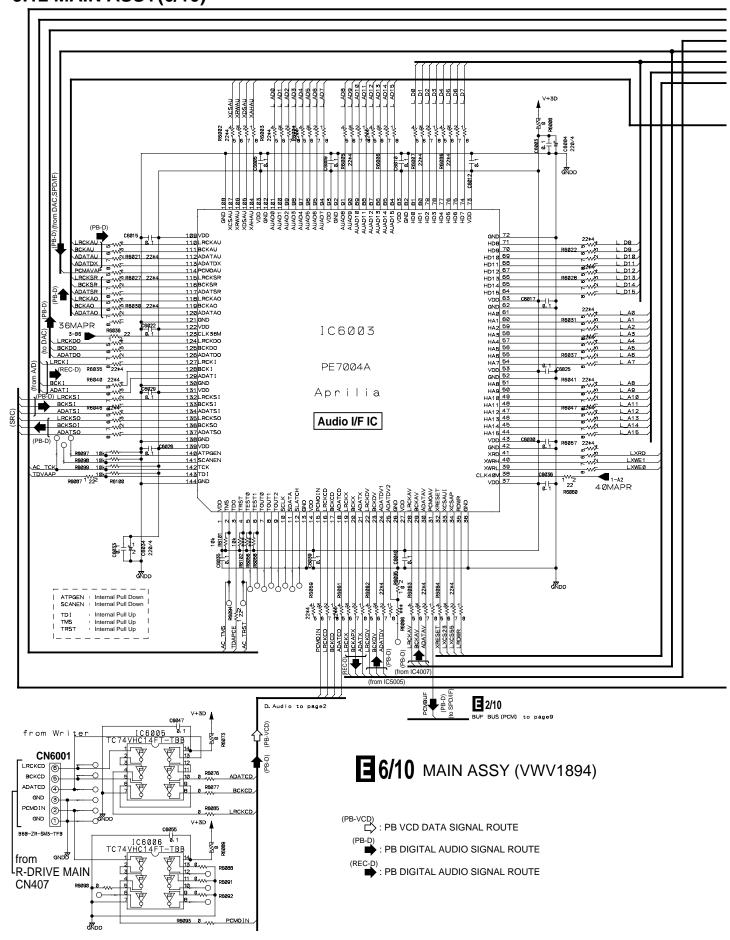
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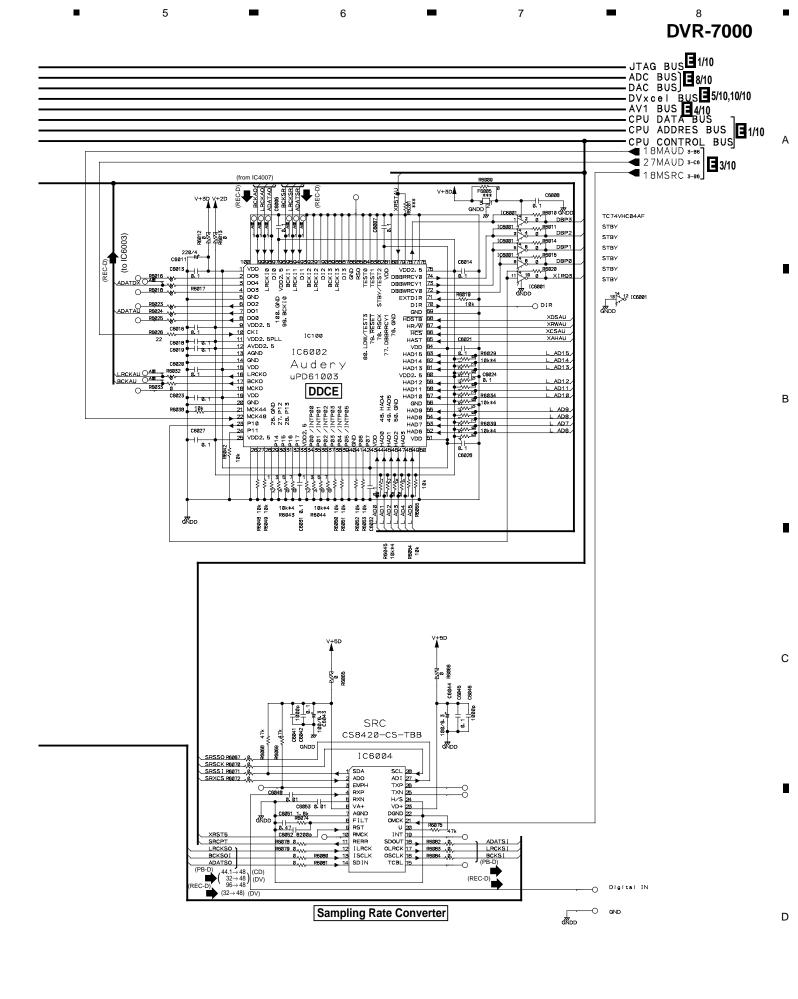
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46 **3**6/10

2 ■ 3 ■

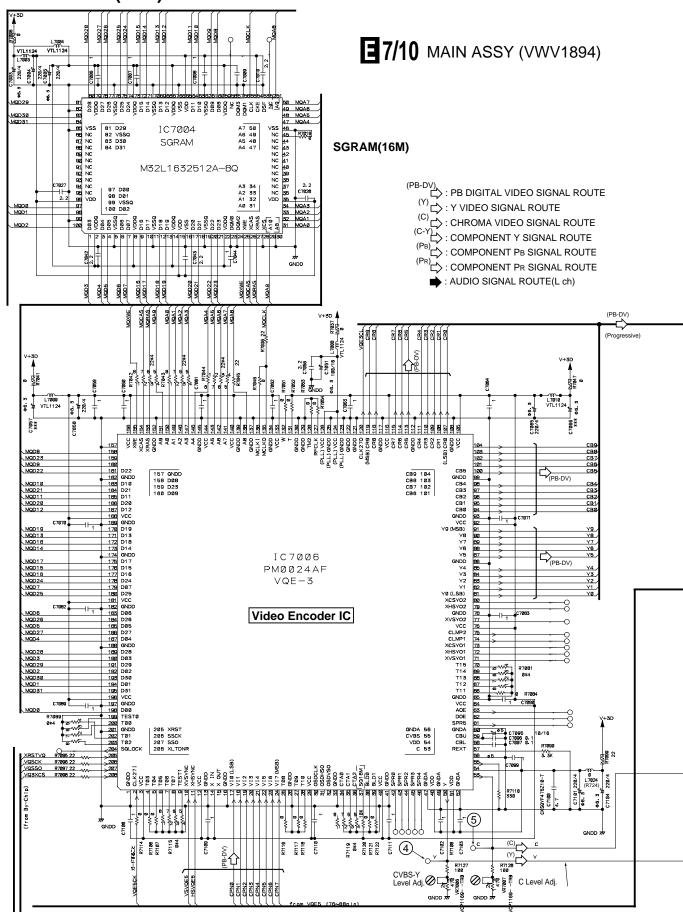


E6/10 47

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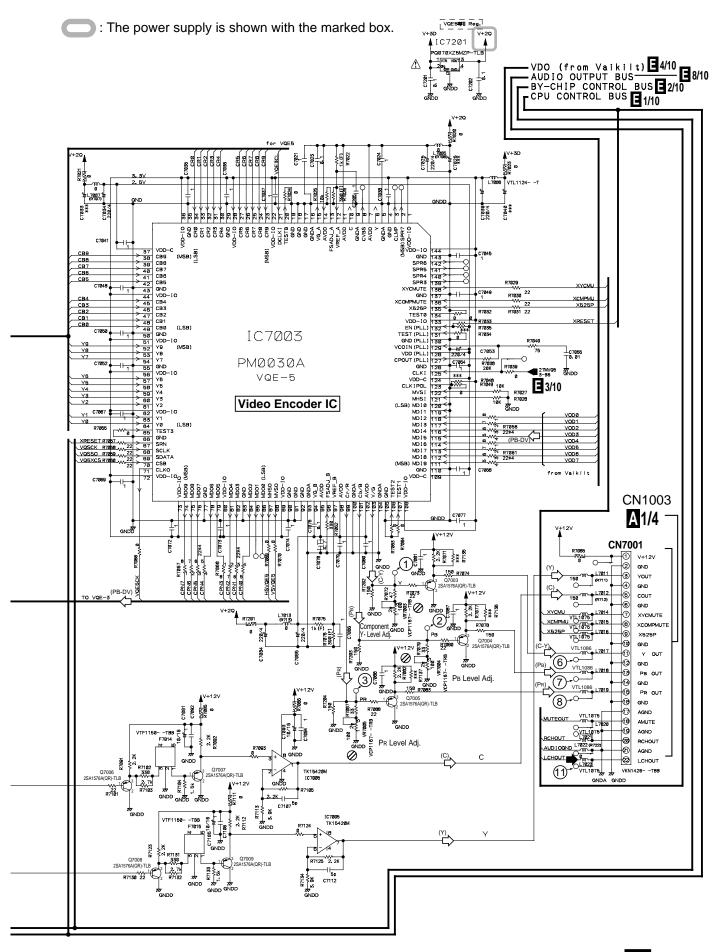
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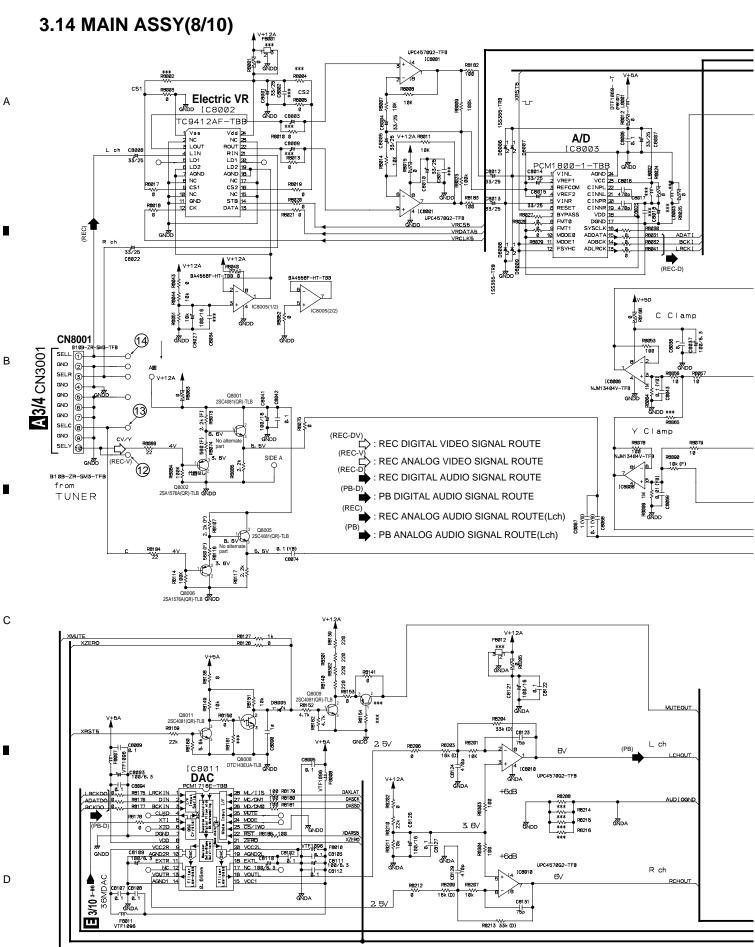
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7/10 49

5

5

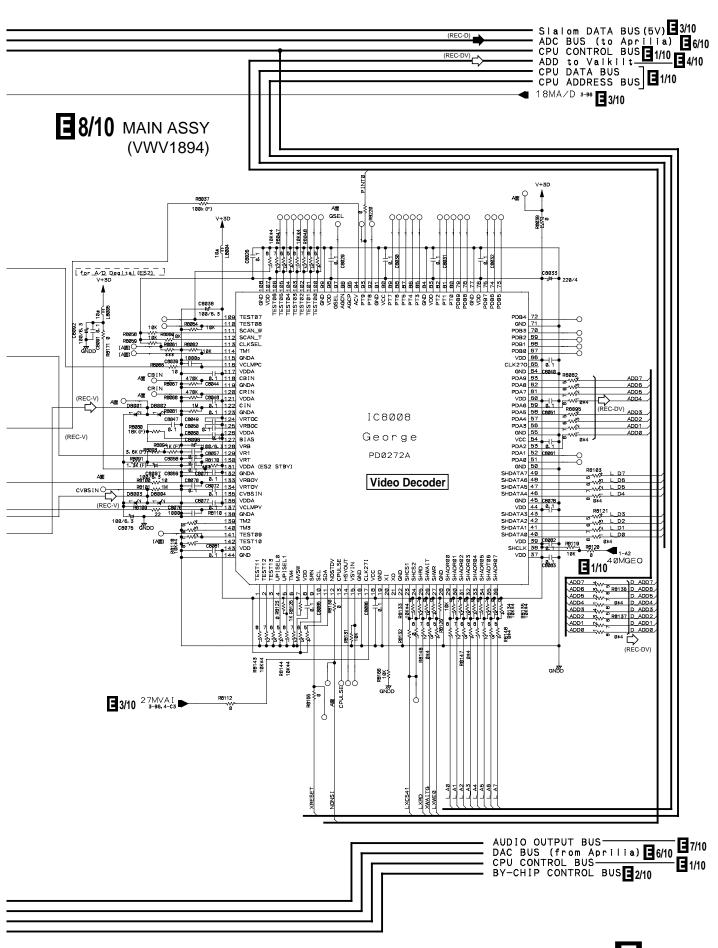
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8/10

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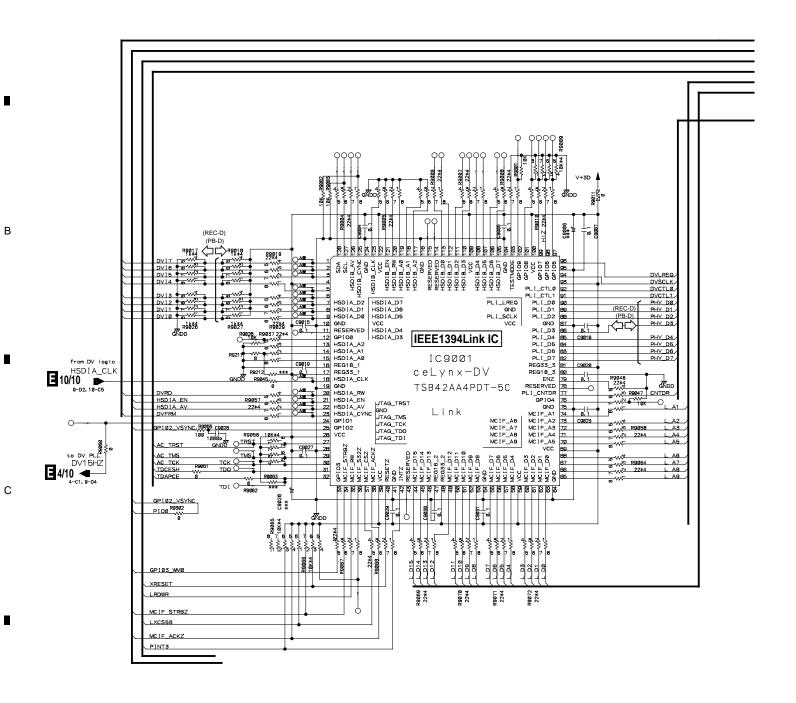
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18/10 51

6 ■

3.15 MAIN ASSY(9/10)

= 9/10 MAIN ASSY (VWV1894)

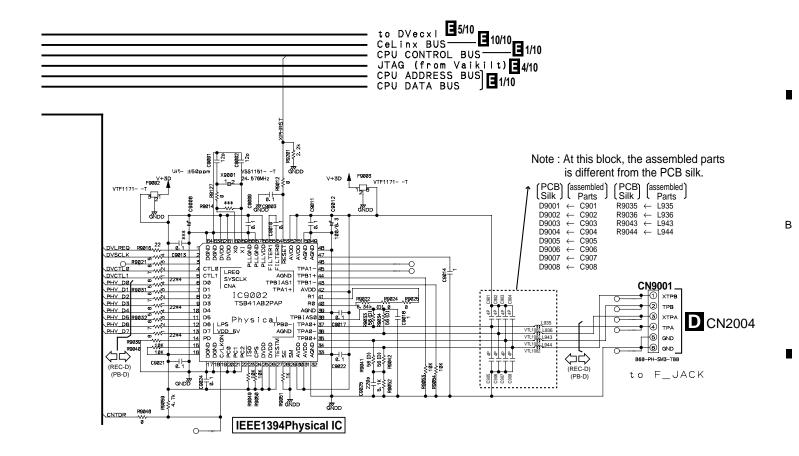


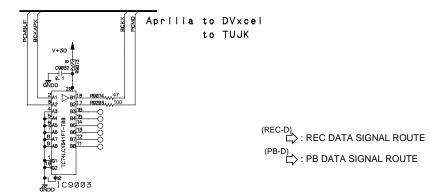
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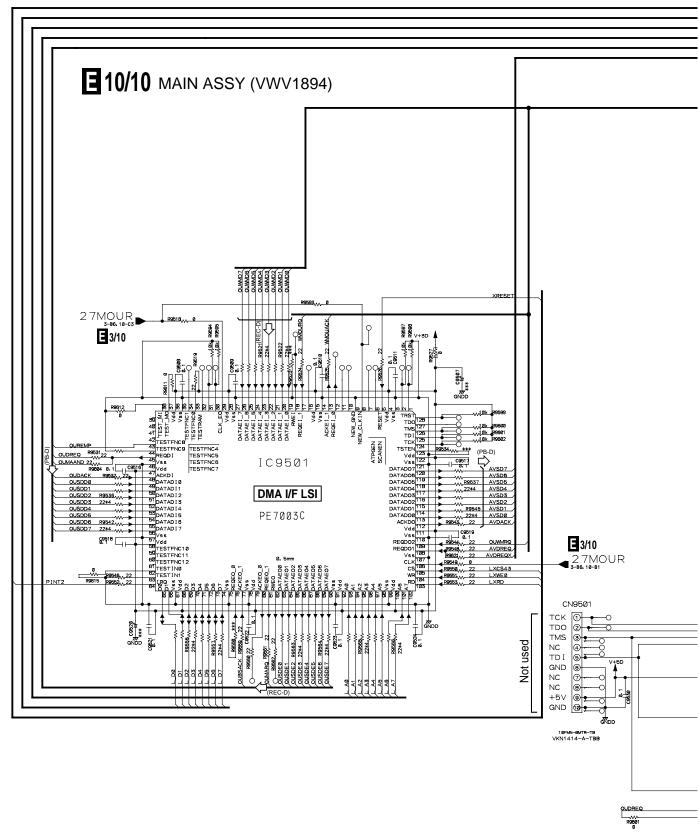




29/10 53

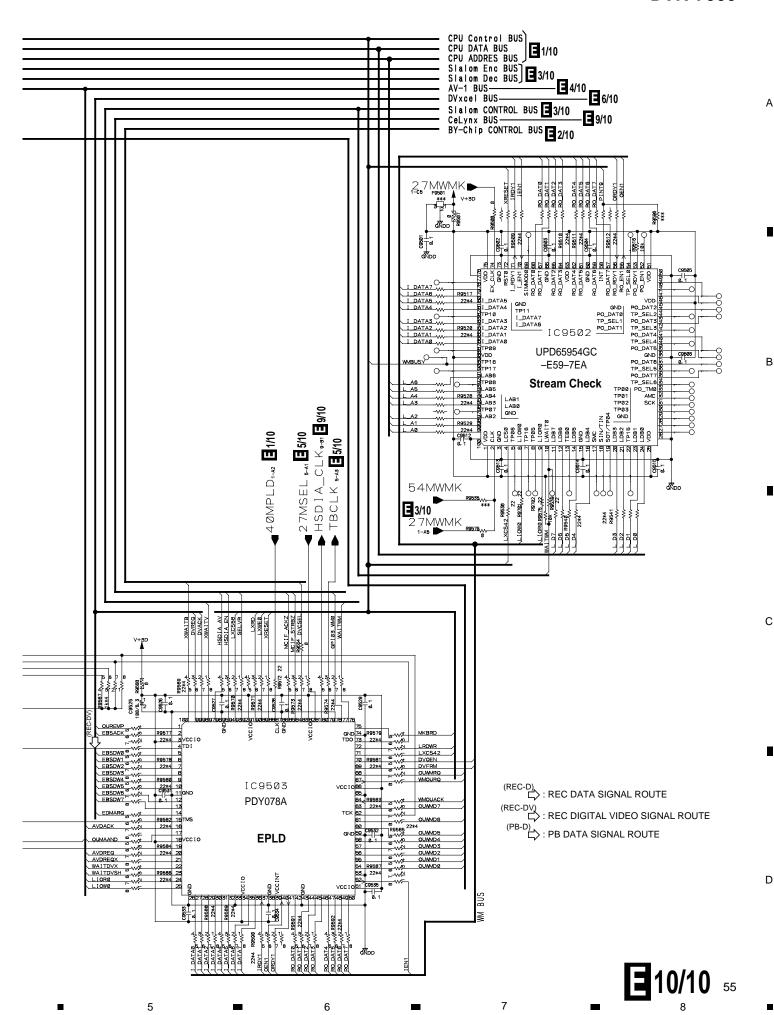
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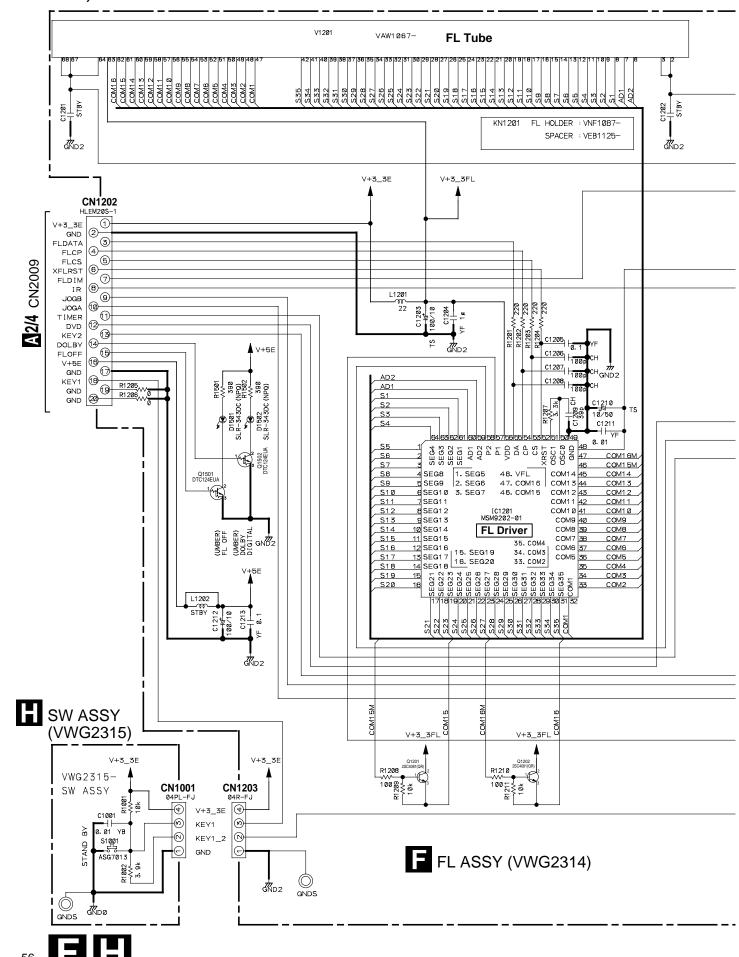
54 10/10

2



С

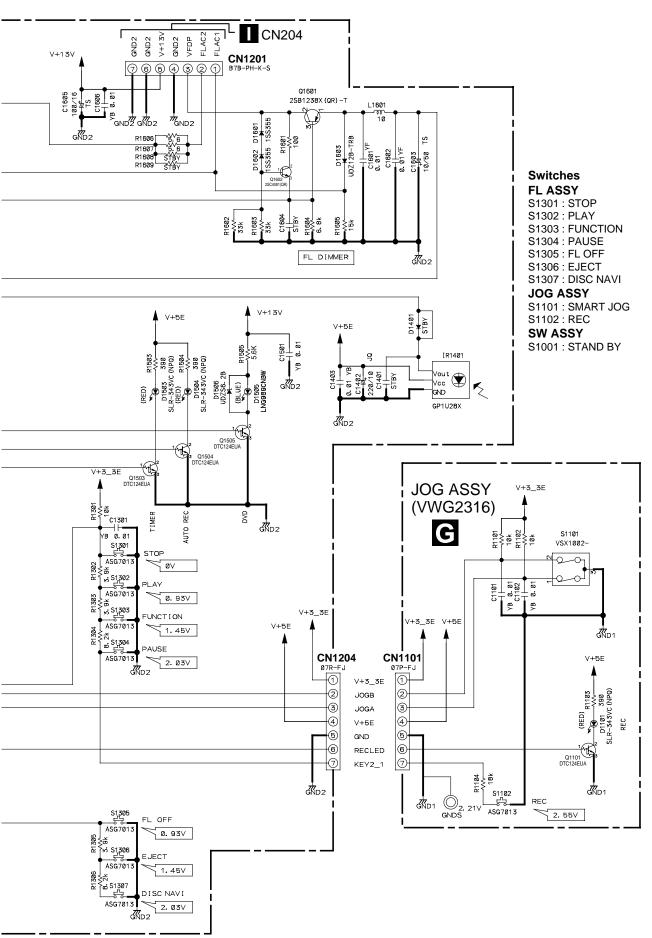
3.17 FL, JOG and SW ASSYS



3

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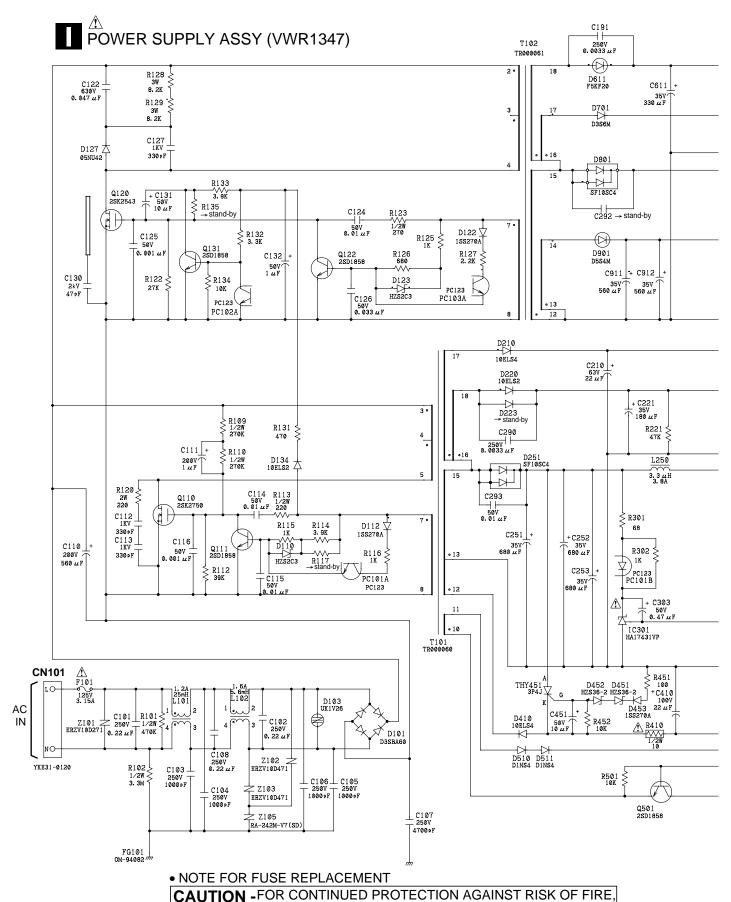
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3.18 POWER SUPPLY ASSY

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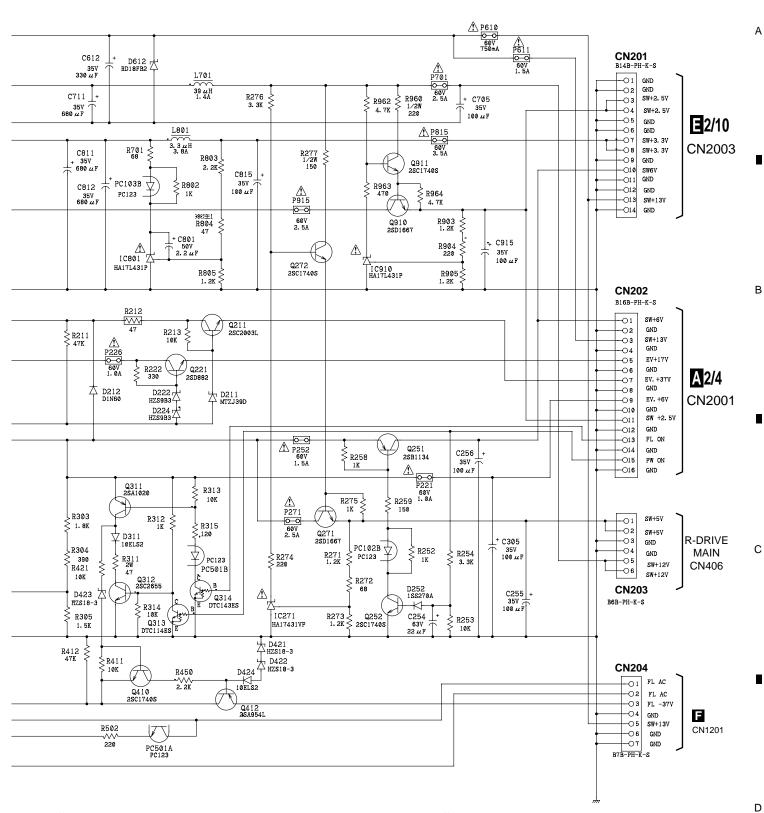
58

2

REPLACE WITH SAME TYPE AND RATINGS OF FUSE

3

-



« NOTE OF SPARE PARTS IN POWER SUPPLY (SYPS) UNIT »

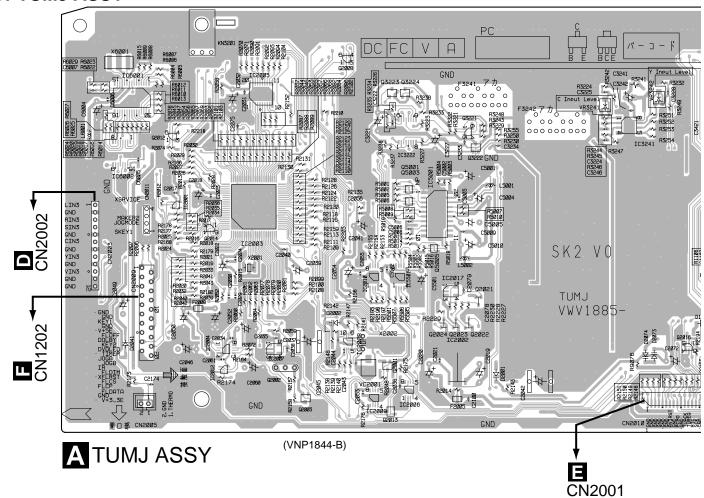
• In case of repairing, use the described parts only to prevent an accident.

• Please write the red \checkmark mark on the board when the primary section of POWER SUPPLY (SYPS) Unit is repaired.

• Please take care to keep the space, not touching other parts when replacing the parts.

4. PCB CONNECTION DIAGRAM

4.1 TUMJ ASSY



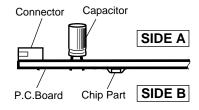
NOTE FOR PCB DIAGRAMS:

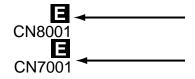
- 1. Part numbers in PCB diagrams match those in the schematic
- diagrams.

 2. A comparison between the main parts of PCB and schematic

diagrams is shown below.				
Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name		
© 0 0 B C E		Transistor		
• ⊙⊙ B C E		Transistor with resistor		
© 0 0 D G S		Field effect transistor		
©00%0000X	***************************************	Resistor array		
000	-	3-terminal regulator		

- 3. The parts mounted on this PCB include all necessary parts for The parts mounted on this FOD include all necessary parts to several destinations.
 For further information for respective destinations, be sure to check with the schematic diagram.
 View point of PCB diagrams.



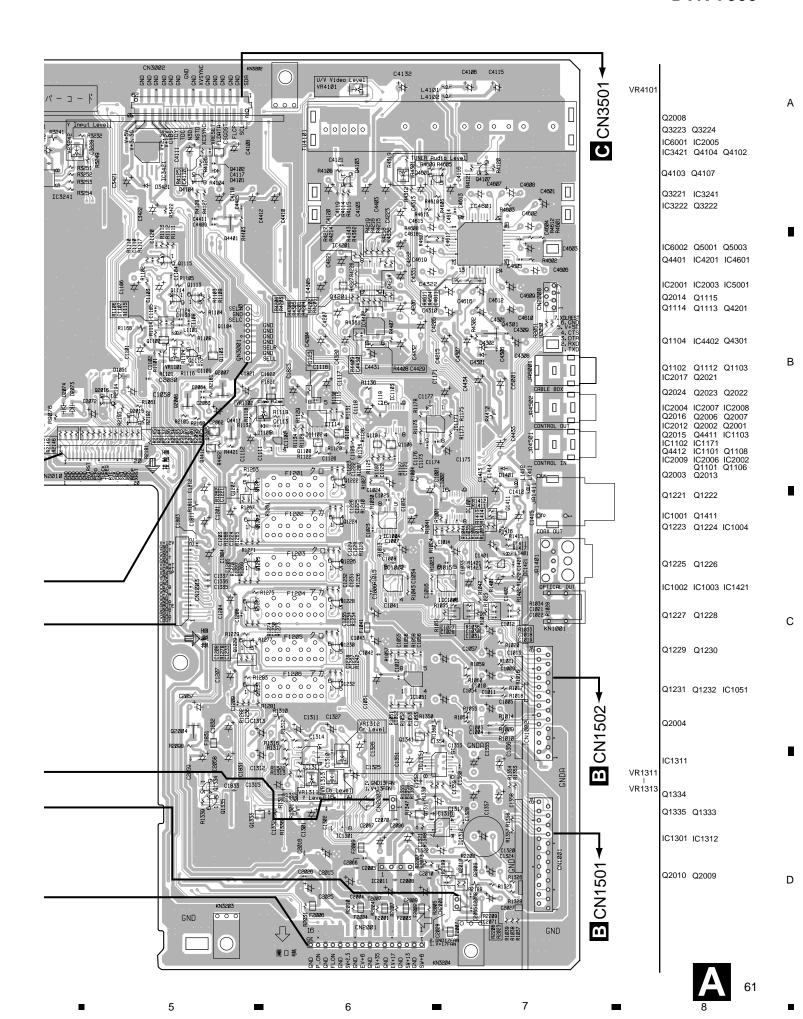


FAN -**MOTOR** FAN **MOTOR**



SIDE A





DVR-7000

Q4112

Q4105

Q6001

TUMJ VWV18 Q4111 Q4110 Q4304 IC4302 IC4202 Q1172 Q1201 Q1203 Q1205 Q1207 Q1209 Q1211 -V- R134Ø ⊣⊢ C1334 IC2013 \bigcirc

Q1342

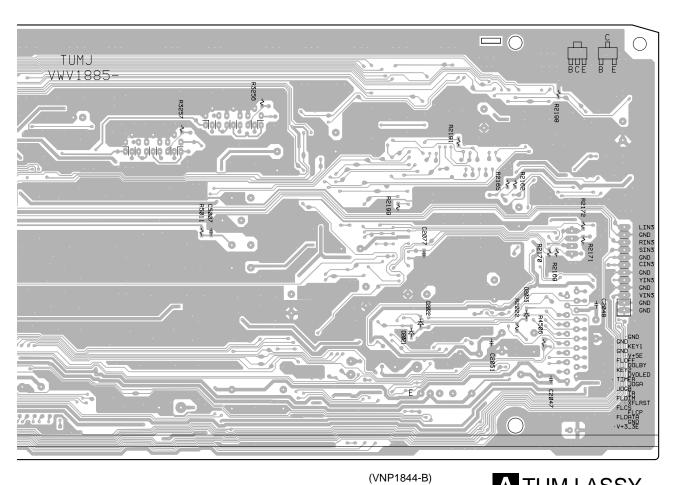
2

DVR-7000

В

С

D



6

5

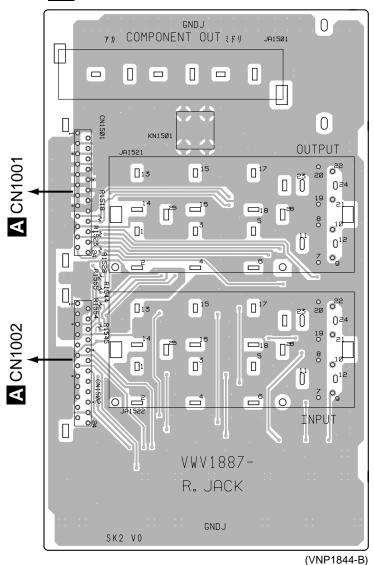
A TUMJ ASSY

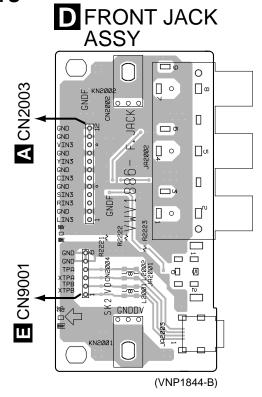
SIDE B

5

4.2 REAR JACK, 3D Y/C and FRONT JACK ASSYS

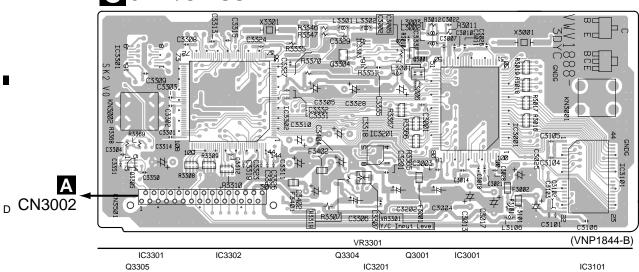
B REAR JACK ASSY





3

C 3D Y/C ASSY



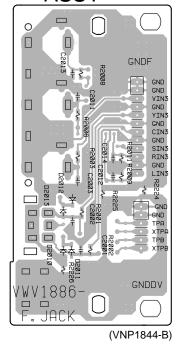
BCD

SIDE A

■ 3

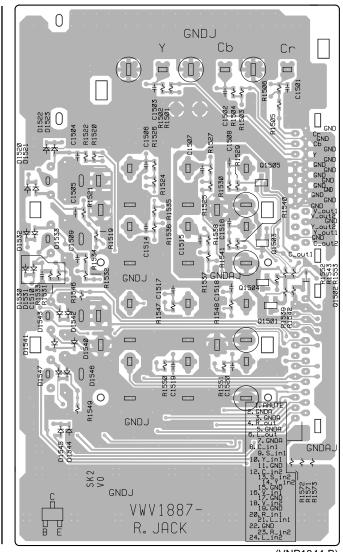
С

D FRONT JACK ASSY



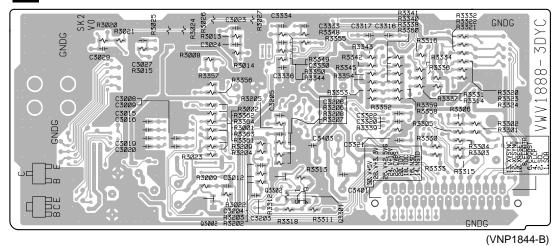
B REAR JACK ASSY

3



(VNP1844-B)

C 3D Y/C ASSY



SIDE B

Q3301

BCD

65

2

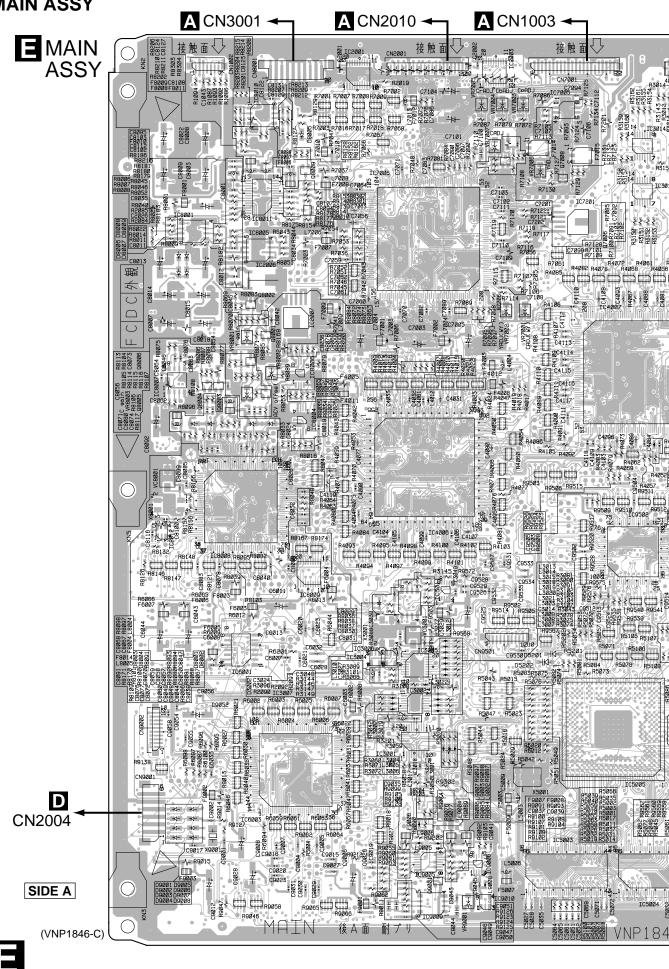
Q3002

Q1505

Q1503

Q1504 Q1502 Q1501

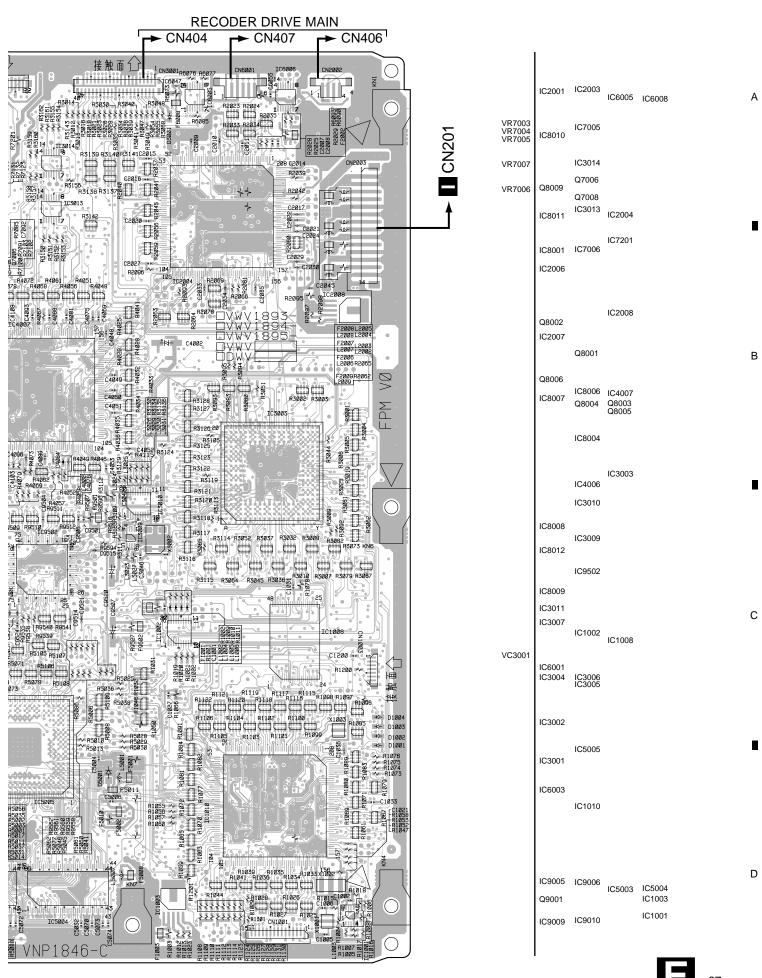
4.3 MAIN ASSY



66

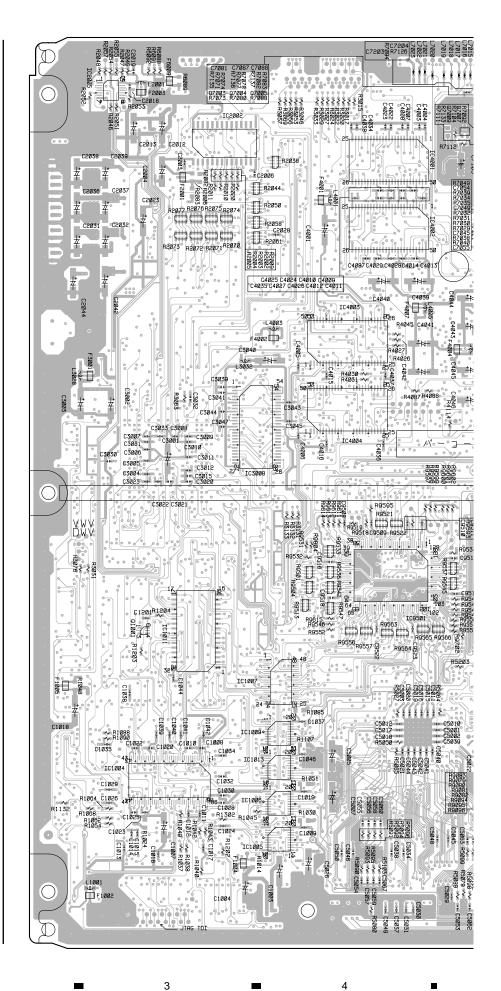
2

DVR-7000



DVR-7000

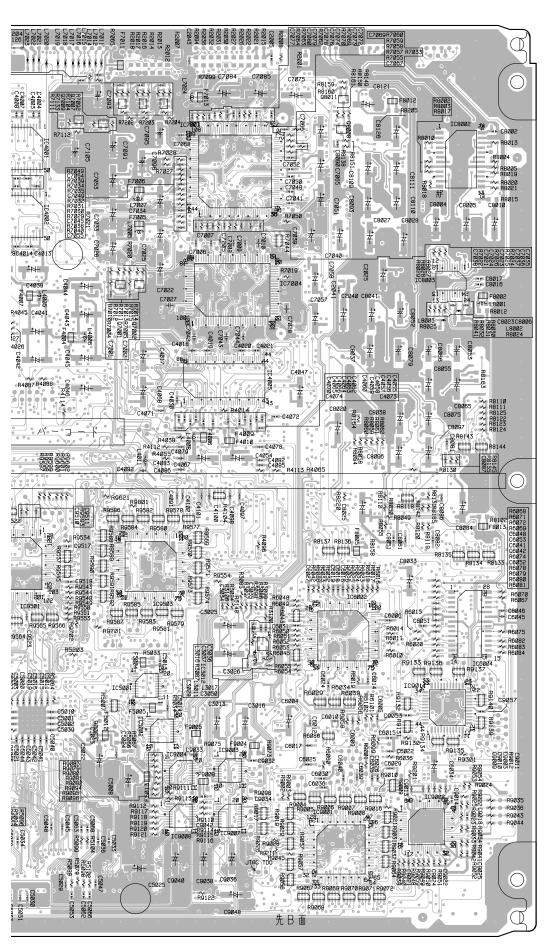
IC2005 Q8011 Q7004 Q7005 Q7003 Q7009 Q7007 Q8008 IC2002 IC4001 IC8002 IC7003 IC4002 Q7001 Q7002 IC7004 IC8003 В IC4003 IC4005 IC4004 IC3008 IC9501 IC9503 С Q1001 IC1011 IC6004 IC6002 IC3012 IC1007 IC5001 IC9011 IC1009 IC5002 IC1013 IC1004 IC9004 IC9003 IC1006 IC9008 IC9007 IC9002 IC1005 D IC9001



3



2



6

5

E MAIN ASSY

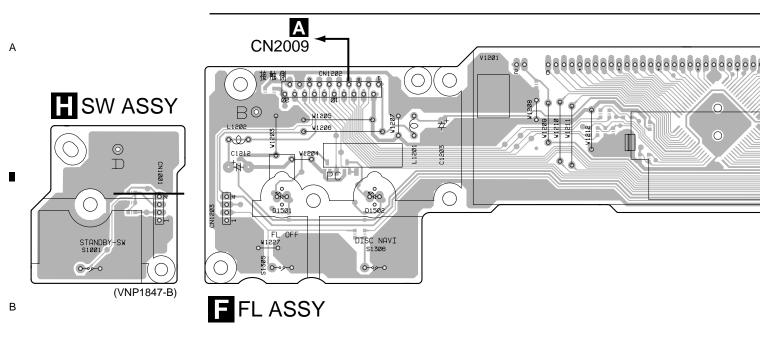
SIDE B

(VNP1846-C)

7

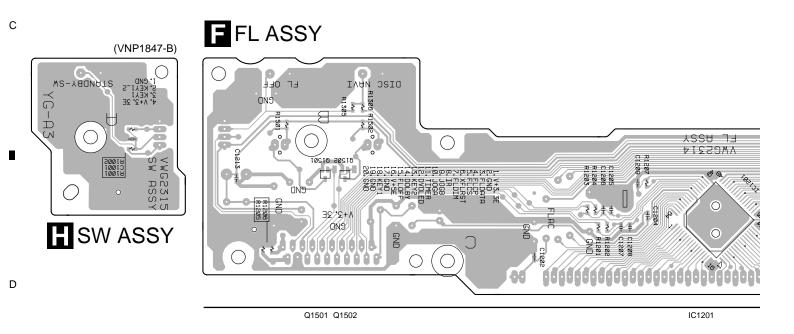


4.4 FL, JOG AND SW ASSYS



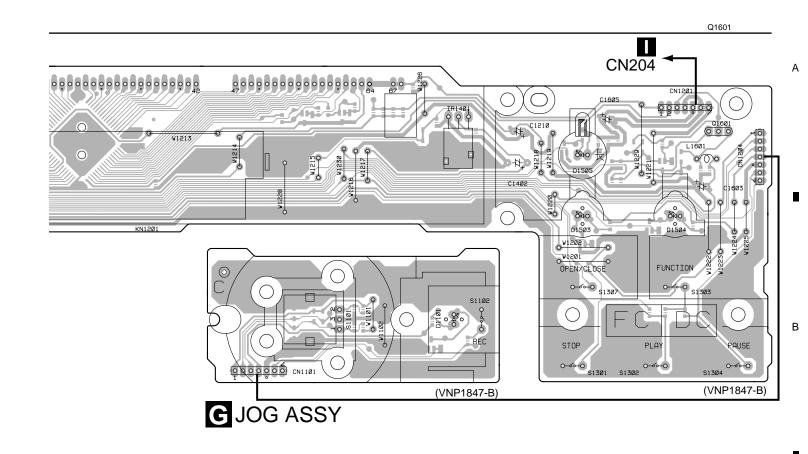
SIDE A

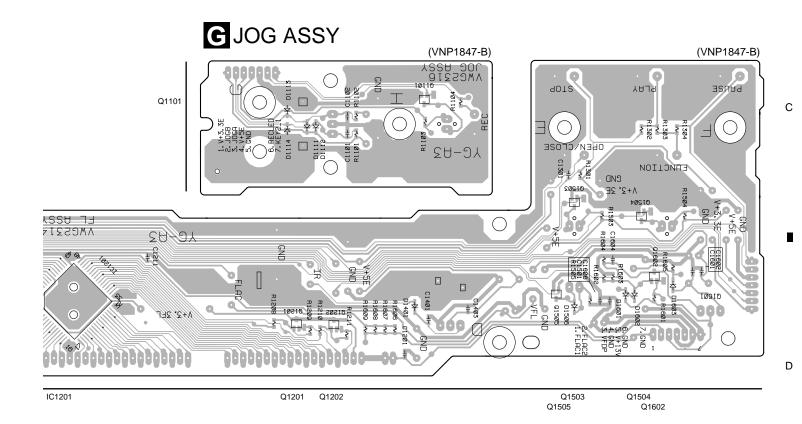
SIDE B



FH

2 3 4

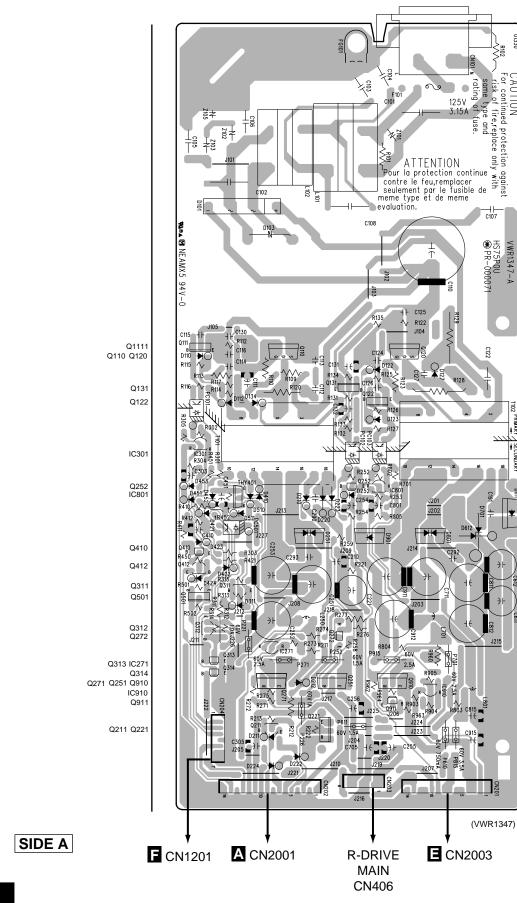




FGH 71

4.5 POWER ASSY

POWER SUPPLY ASSY



D

2

3

Part No.

5. PCB PARTS LIST

Description

Mark No.

NOTES: • Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.

- The \triangle mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- When ordering resistors, first convert resistance values into code form as shown in the following examples.

Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

Mark No.

Description

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).

Part No.

	ite: Decempaten		mark Hor Boodinphion	
	OF ACCEMBLIES		Q1207,Q1209,Q4110	2SA1576A
LIST	OF ASSEMBLIES		Q2006,Q4411	2SB1132
	TILLID ACCOV	\/\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Q2002	2SB1237X
	TUJB ASSY	VWM2103		
	⊢TUMJ ASSY	VWV1885	Q1311,Q1411,Q2023,Q3222,Q4	102 2SC4081
	REAR JACK ASSY	VWV1887	Q2004,Q2007,	
	- 3D Y/C ASSY	VWV1888		
	FRONT JACK ASSY	VWV1886	Q2009,Q2010,Q2022	2SD2114K
	- FRONT JACK ASST	V VV V 1000	Q1104	2SK210
	MAIN ASSY	VWV1894	Q1105,Q1108,Q2001,Q2021	DTA124EUA
			Q1172,Q1333,Q1341,Q2013,Q2	2024 DTC124EUA
	FLKB ASSY	VWM2105	Q3223	DTC124EUA
	⊢ FL ASSY	VWG2314		
			Q2003,Q2005,Q4412	DTC142E11A
	⊢ JOG ASSY	VWG2316		DTC143EUA
	└─ SW ASSY	VWG2315	Q1101,Q1113,Q1221–Q1232,Q	
			Q3221,Q4103,Q4104	HN1B01FU
Δ	POWER SUPPLY ASSY	VWR1347	Q1112,Q1114,Q1115,Q2008	HN1K03FU
4.5	1 OWER COLLET MOOL	V VVICTO-17	Q2012,Q2015,Q4601	HN1K03FU
			Q2012,Q2013,Q4001	THVIROSIO
Δ	TUMJ ASSY		Q4201,Q5001,Q5003,Q5005	RN1903
	I OIVIJ AGG I		Q2014	RN2903
OE NAI	CONDUCTORS		D2003	1SR154-400
SEIVII	CONDUCTORS		D2001,D2002,D2073,D2074	EP10QY03
	IC2002	BA033FP		
	IC2013	BA10393F	D1101,D1401,D2021-D2023,D2	2041 MATTI
	IC4402	BA4558F-HT	D4302,D4501	MA111
	IC1102	BA7046F	D4101	UDZ33B
	IC1351	BA7665FS	D4301	UDZS9.1B
			D4301	UDZ39.1B
	IC2010 IC5501	BD2/E16EV		
	IC2010,IC5501	BR24E16FV	COILS AND FILTERS	
	IC3222,IC4201	BU4052BCFV	COILS AND FILTERS	
			COILS AND FILTERS L1401,L1412,L5001,L5002	LCTA100J2520
	IC3222,IC4201	BU4052BCFV		
	IC3222,IC4201 IC4601 IC5001	BU4052BCFV CXA2094Q LC7454M	L1401,L1412,L5001,L5002 L1101	LCTA330J2520
	IC3222,IC4201 IC4601	BU4052BCFV CXA2094Q	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32	LCTA330J2520 42 VTF1166
	IC3222,IC4201 IC4601 IC5001 IC1002	BU4052BCFV CXA2094Q LC7454M MM1114XF	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205	LCTA330J2520 42 VTF1166 VTF1167
	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32	LCTA330J2520 42 VTF1166
	IC3222,IC4201 IC4601 IC5001 IC1002	BU4052BCFV CXA2094Q LC7454M MM1114XF	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205	LCTA330J2520 42 VTF1166 VTF1167
^	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007-F2009	LCTA330J2520 42 VTF1166 VTF1167 VTF1170
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205	LCTA330J2520 42 VTF1166 VTF1167
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007-F2009 L4101,L4102	LCTA330J2520 42 VTF1166 VTF1167 VTF1170
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007-F2009 L4101,L4102	LCTA330J2520 42 VTF1166 VTF1167 VTF1170
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102	LCTA330J2520 42 VTF1166 VTF1167 VTF1170 VTL1096
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286	LCTA330J2520 42 VTF1166 VTF1167 VTF1170 VTL1096 CCSRCH100D50
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286	LCTA330J2520 42 VTF1166 VTF1167 VTF1170 VTL1096 CCSRCH100D50
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32: F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115	LCTA330J2520 42 VTF1166 VTF1167 VTF1170 VTL1096 CCSRCH100D50 CCSRCH101J50 CCSRCH101J50 CCSRCH101J50 CCSRCH102J50
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2009 IC2005	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9 C1113	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2005 IC1101	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2GU04HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT TC7WH123FU	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9 C1113 C1107	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2009 IC2005	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9 C1113 C1107 C4502	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2005 IC1101	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2GU04HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT TC7WH123FU	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9 C1113 C1107	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2005 IC1101 IC3241	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT TC7WH123FU TK15420M	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9 C1113 C1107 C4502	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2005 IC1101 IC3241 IC1311	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT TC7WH123FU TK154520M TK15452V	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007–F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281–C2286 C1335–C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9 C1113 C1107 C4502	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2005 IC1101 IC3241 IC1311	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT TC7WH123FU TK15420M TK15452V	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007—F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281—C2286 C1335—C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9 C1113 C1107 C4502 C4325,C4334 C5007	LCTA330J2520 42 VTF1166
Δ	IC3222,IC4201 IC4601 IC5001 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2005 IC1101 IC3241 IC1311 IC1312 IC4202,IC4302	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT TC7WH123FU TK15420M TK15452V TK15453V UPC4570G2	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007—F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281—C2286 C1335—C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9.C1113 C1107 C4502 C4325,C4334 C5007 C1351,C5005	LCTA330J2520 42 VTF1166 VTF1167 VTF1170 VTL1096 CCSRCH100D50 CCSRCH101J50 CCSRCH101J50 CCSRCH102J50 CCSRCH120J50 CCSRCH220J50 CCSRCH220J50 CCSRCH220J50 CCSRCH220J50 CCSRCH390J50 CCSRCH470J50 CCSRCH681J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50
Δ	IC3222,IC4201 IC4601 IC5001 IC1002 IC1003,IC1004,IC1171 IC2003 IC2011 IC2017 IC2007 IC2008 IC1421,IC2001,IC2012 IC2006 IC2004 IC1001,IC1301 IC2009 IC2005 IC1101 IC3241 IC1311	BU4052BCFV CXA2094Q LC7454M MM1114XF MM1118XF PE5275B9 PQ12RF11 PST9120N PST9130N RV5C386A SN74AHC1G08HDCK SN74AHC2G126HDCT SN74AHC2GU04HDCT SN74LV4053APW TC4W53FU TC74VHCT541AFT TC7WH123FU TK15420M TK15452V	L1401,L1412,L5001,L5002 L1101 F1202,F1204,F1206,F3241,F32 F1201,F1203,F1205 F1821,F1831,F2007—F2009 L4101,L4102 CAPACITORS C1120,C2043,C2281—C2286 C1335—C1337,C2029,C2030 C4150,C4151 C1003,C1010,C1035,C1115 C1108,C1124 C4202,C4216,C4303,C4333,C9 C1113 C1107 C4502 C4325,C4334 C5007	LCTA330J2520 42 VTF1166 VTF1167 VTF1170 VTL1096 CCSRCH100D50 CCSRCH101J50 CCSRCH101J50 CCSRCH102J50 CCSRCH120J50 CCSRCH220J50 CCSRCH220J50 CCSRCH220J50 CCSRCH2821J50 CCSRCH470J50 CCSRCH681J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50 CCSRCH821J50

Mark	No.	Description	Part No.	Mark	No.	Description F	Part No.
	C4615		CEANP4R7M50			,C1310,C1314,C1316,C1321	CKSRYF105Z10
		C4108,C4111,C4118,C4132	CEAT100M50			,C1353,C1360,C1413,C2059	CKSRYF105Z10
	C4205-	-C4207,C4221-C4223,C4320	CEAT100M50		C2077		CKSRYF105Z10
	C4331,		CEAT100M50			,C2045 (1.0F/5.5V)	PCH1132
	C1001,	,C1014,C1024,C1112	CEAT101M10		C4601	(10μF/50V)	VCH1224
	C1117,	,C1118,C1175,C1201,C1204	CEAT101M10		C4603	(3.3µF/50V)	VCH1225
		C1301,C1311,C1317,C1354	CEAT101M10				
		,C1402,C1821,C1831,C2009	CEAT101M10	RESI	STORS	:	
		-C2020,C2022,C2032,C2035				,R1166,R1301,R1310,R1330	RS1/10S0R0J
	C2041,	,C2049,C2054,C2057,C2058	CEAT101M10		R1350	,R2188,R2189,R3241,R4410	RS1/10S0R0J
	C2060.	C2062,C2072,C4103,C4106	CEAT101M10		R1115		RS1/16S1501F
		C4116,C4120,C4410,C4412	CEAT101M10			,R3252	RS1/16S1801F
	C4432	C5004,C5010,C5501	CEAT101M10		R1348	,R3244,R3251	RS1/16S2201F
		,C1101,C1103,C1106,C1804	CEAT101M16		DAGE	,R1257,R1259	RS1/16S2701F
	C1811,	,C1812,C2006,C2007,C3221	CEAT101M16			,R1205,R1221,R1222	RS1/16S2701F RS1/16S3300F
	C3227	C3241,C4215,C4301,C4305	CEAT101M16		R1237	,R1238	RS1/16S3300F
		,C4310,C4403,C4431,C4433	CEAT101M16		R1201	,R1206,R1217,R1223,R1233	RS1/16S3301F
	C2004,		CEAT101M25		R1239		RS1/16S3301F
	C1320	,	CEAT102M6R3		_		
	C1005,	,C1009,C1012,C1013	CEAT1R0M50		R1347		RS1/16S3901F
						,R1215,R1225,R1231,R1241 ,R3246,R3248,R3253,R3255	RS1/16S4700F RS1/16S4700F
		,C1033,C1171,C4608,C4619	CEAT1R0M50			,R1258,R1260,R3256,R3257	RS1/16S5601F
	C1356,		CEAT220M25		R4604		RS1/16S6202F
		,C1325,C1326,C1414	CEAT221M6R3		114004		1101/10002021
	C5001	,C1057,C1312,C1313,C1327	CEAT2R2M50 CEAT470M16		R1010	,R1014,R1016,R1018	RS1/16S75R0F
	C 1034,	,01037,01312,01313,01327	CEATATOWITO			,R1021,R1041-R1043	RS1/16S75R0F
	C1415		CEAT470M16		R1108		RS1/16S8200F
	C2067		CEAT471M16			1–VR1313,VR4101 (1kΩ)	ACP1089
	C1322,	C1324,C1355,C1357,C1832	CEAT471M6R3		Other	Resistors	RS1/16S□□□J
	C4609,		CEAT4R7M50				
	C4105,	,C4107,C4114,C4121	CKSRYB102K50	OTHE	ERS		
	C1006	,C1016,C1023,C1176,C1412	CKSRYB103K50			(32kHz)	VSS1143
		,C3225,C3228,C4110,C4117	CKSRYB103K50			(6.25MHz)	VSS1162
	C4319.		CKSRYB103K50		CN200		12PL–FJ B10B–ZR
		C1011,C1034,C1105,C1318	CKSRYB104K16		CN200		B16B-PH-K
	C1352,	,C1359,C3224,C3246	CKSRYB104K16		011200	or Connector	DIOD III K
	04040	04222	CKCDVD405KCD0		JA140		GP1FA551TZ
	C1319, C4618	,01323	CKSRYB105K6R3 CKSRYB123K50		CN200		HLEM20S-1
	C4605		CKSRYB272K50			06,CN2007 Plug 2P	KM200SA2
	C4318.		CKSRYB472K50			1,JA4502 Jack	RKN1004
	C4604		CKSRYB473K25		JA141	1 Jack	VKB1074
	04047		OKODYDEOOKEO		CN200	08 7P Connector	VKN1267
	C4617	,C1008,C1015,C1025,C1102	CKSRYB562K50 CKSRYF104Z25			01,CN1002 B to B Connector 24F	
		,C1109–C1111,C1116,C1119				0 20P Connector	VKN1424
		,C1122,C1125,C1126	CKSRYF104Z25		CN100		VKN1426
		C1174,C1177,C1202,C1203	CKSRYF104Z25		CN300	2 Connector	VKN1626
	C400F	C1206 C1209 C1200 C1201	CK6DVE404705		1001	Screw Plate	VNE1948
		,C1206,C1208,C1209,C1221 ,C1224,C1226,C1227	CKSRYF104Z25 CKSRYF104Z25			1-KN3204 Earth Metal Fitting	VNF1084
		,C1230,C1232,C1233	CKSRYF104Z25		4101	TV Tuner Pack (USA)	VXF1005
		,C1236,C1238,C1302,C1403	CKSRYF104Z25				
		C1803,C1822,C1833,C2005	CKSRYF104Z25	Б		LACK ACCV	
	00000	00040 00047 00004	01/00/15404705	D	KEAK	JACK ASSY	
		,C2010,C2017,C2021 ,C2024,C2028,C2031	CKSRYF104Z25 CKSRYF104Z25	SEMI	COND	UCTORS	
		,C2024,C2026,C2031 ,C2034,C2036–C2038,C2040		U	Q1502		2SA1576A
		,C2047,C2048,C2051,C2053	CKSRYF104Z25			,Q1503-Q1505	2SD2114K
		C2061,C2063–C2066	CKSRYF104Z25		4.00.	, 4.000 4.000	
	0	00074 00070 00070	0//00//=:	RESI	STORS	3	
		-C2071,C2073,C2078-C2080				,R1503,R1505,R1519,R1520	RS1/16S75R0F
		,C3233,C3234,C3242,C4104	CKSRYF104Z25			,R1531,R1532,R1535	RS1/16S75R0F
		,C4119,C4131,C4201,C4203 ,C4214,C4304,C4306,C4309	CKSRYF104Z25 CKSRYF104Z25			Resistors	RS1/16S□□□J
		,C4409,C4411,C4425	CKSRYF104Z25				
	0.011,	, = 1.30, 0 1.1., 0 1.120		ОТНЕ	ERS		
		,C4430,C4501,C4611,C5003	CKSRYF104Z25		JA150	1 3P Pin Jack	VKB1115
	C5009,	,C5502	CKSRYF104Z25			1,JA1522 Jack	VKB1173

/lark	No.	Description F	Part No.	Mark	No.	Descri	ption	Part No.
	CN150	1,CN1502 B to B Connector 24F	P VKN1392		JA2003		DV-Terminal	VKB1171
	1501	Screw Plate	VNE2247		KN2001	,KN2002	Earth Metal Fitting	VNF1084
2				П				
5	3D Y/C	ASSY			/AIN /	ASSY		
ЕМІ	CONDU	ICTORS		SEMIC	CONDU	CTORS		
	IC3101		MSM514265C-60TS	\triangle	IC2006			BA178M05FP
	IC3201		TK15420M		IC8005			BA4558F-HT
	IC3001 Q3002		UPD64082GF-3BA 2SA1576A		IC6004 IC5005			CS8420-CS DVXCEL-BA1
	Q3002 Q3001		2SC4081		IC1010			HD6417709AF100B
	Q3301 Q3305		HN1B01FU HN1K03FU		IC3008 IC1004			HY57V641620HGT-7 K4S643232E-TC60
	Q3303		THATROST O		IC7004			M32L1632512A-8Q
OIL	SAND	FILTERS			IC4003,	IC4004		M5M4V18165DTP-68
O.L.	L3003	. IETEKO	LCTA150J2520		IC4007			M65774AFP
		F3002,F3101	VTF1170		IC4001			MB81F161622C-80F
		_9002,L9023,L9301,L9302	VTL1081		IC4001			MB81F643242B-70
	L3001,I	_3106	VTL1096		IC2002			MSM514800C-60JS
	. 				IC8006			NJM13404V
APA	CITOR	S	000000000		IC3007			NJM2115M
	C3337 C3350.	C3351	CCSRCH100D50 CCSRCH101J50		IC8011			PCM1716E
	C3350,		CCSRCH101J50 CCSRCH151J50		IC8003			PCM1800-1
	C3027,		CCSRCH180J50		IC8008			PD0272A
	C3013		CEAT100M50		IC4006 IC9503			PD6342A PDY078A
	C3017,	C3025	CEAT101M10		109303			IDIOTOA
	C3006,		CEAT471M6R3		IC2004			PE5108A
	C3305		CEJQ101M6R3		IC3003			PE5219A
	C3202		CEV101M16		IC9501 IC6003			PE7003C PE7004A
	C3004		CEV221M4		IC3001			PLL1700E
	C3103		CKSRYB102K50		107000			D14000445
		-C3009,C3014-C3016	CKSRYB104K16		IC7006 IC7003			PM0024AF PM0030A
	C3019,		CKSRYB104K16	\triangle	IC1003,	IC2008		PQ070XZ5MZP
		C3201,C3304,C3307 C3003,C3005,C3010,C3011	CKSRYF104Z25 CKSRYF105Z10	$\overline{\Delta}$	IC2007			PQ12DZ51
	00001,	00000,000000,00010,00011	01(01(11 100210	Δ	IC7201			PQ2TZ15
		C3026,C3028,C3102	CKSRYF105Z10		IC3011			SN74AHC2G53HDCT
	C3104,	C3105	CKSRYF105Z10		IC1011			TC554001AFT-70V
-01	07000				IC5003,			TC59S6432CFT-80
ESI	STORS	D0040	DAD404041		IC1007			TC74LCX16245AFT
	R3016- R3307	-K3U19	RAB4C101J RS1/10S0R0J		iC1002,	iC1005,IC	C1006,IC1009	TC74LCX541FT
	R3204,	R3207	RS1/16S1501F		IC1013.	IC2001,IC	3005	TC74LCX541FT
	R3206		RS1/16S2201F		IC3010,	IC9003		TC74LCX541FT
	Doors		D04/46007017			IC6005,IC	26006	TC74VHC14FT
	R3203	1 (470Ω)	RS1/16S2701F ACP1088		IC3013 IC3014			TC74VHCT08AFT TC74VHCT32AFT
		(47002) Resistors	RS1/16S□□□J		103014			I O I 4 V II O I 3 Z A F I
					IC2003			TC74VHCT541AFT
THE	ERS				IC3002			TC74VHCU04FT
		(20.000MHz)	ASS7023		IC3012 IC3004,	IC3006		TC7SH04F TC7SLU04F
	CN350	1 B to B Plug 30P	VKN1797		IC3004,	100000		TC7SLU04F TC7WU04FU
	3001,30	002 Screw Plate	VNE2247					
					IC8002			TC9412AF
٦,	EDON!	T JACK ASSY			IC7005 IC9002			TK15420M TSB41AB2PAP
	LKON	1 JACK 4991			IC9002			TSB42AB4PDT
ESI	STORS				IC8001,	IC8010		UPC4570G2
	Other F	Resistors	RS1/16□□□J		IC6002			UPD61003
					IC6002			UPD65954GC-E59-7
THE	ERS				IC1008			VYW1898
	CN200		12R-FJ				8002,Q8006	2SA1576A
	CN2004		B6B-PH-K		Q8001,0	Q8005,Q8	8008	DTC124EUA
	JA2001 JA2002		VKB1169 VKB1170		Q1001			HN1K03FU
	U/12002	. Jaok	VINDI I I O		w 1001			1114111001 0

Mark	No.	Description	Part No.	Mark	No.	Description F	Part No.
	D8001	-D8009	1SS355		C8043	3,C8068,C8074	CKSRYB104K16
	D5001		EC10QS04		C8067	,	CKSRYB105K6R3
		,D5202	EP10QY03		C6052		CKSRYB822K50
	D3002		KV1832E			,C1002,C1008-C1013	CKSRYF104Z25
					C1016	6,C1017,C1019–C1044,C1046	CKSRYF104Z25
COIL		FILTERS			C1200),C2001-C2003,C2006	CKSRYF104Z25
		F2101,F3101-F3103	DTF1069			-C2011,C2014-C2022,C2024	
		-F3112,F3117,F3124,F3127	DTF1069		C2026	6-C2030,C2033-C2035,C2041	CKSRYF104Z25
	F3132,	F2062,F2065,F2102–F2105	DTF1070 DTF1070			5,C3004–C3012,C3014,C3015	CKSRYF104Z25
		F4103-F4106,F5106,F5107			C3017	'-C3024,C3027-C3034,C3039	CKSRYF104Z25
	L8004.	1 9005	LCYA100J2520			-C3050,C4004,C4008,C4010	CKSRYF104Z25
	L3016	L8003	LCYA1R2J2520			3-C4021,C4023,C4025	CKSRYF104Z25
		F8008,F7014,F7015	VTF1150			0-C4034,C4048-C4053 5-C4066,C4069-C4086	CKSRYF104Z25 CKSRYF104Z25
		-F2009,F4006,F4010-F4012				3–C4006,C4069–C4066 3–C4118,C5001–C5004,C5006	
	F5002,	F5009,F5011-F5013	VTF1171		04000	0 04110,03001 03004,03000	01(01(11 104220
	F9002.	F9003	VTF1171			0,C5010,C5016,C5018	CKSRYF104Z25
		-L7016,L7020,L7021,L7023	VTL1075			3,C5024,C5027–C5040,C5043 5–C5050,C5069–C5074,C6003	CKSRYF104Z25 CKSRYF104Z25
	L1004,		VTL1078		C6005	5-C6010,C6012-C6033	CKSRYF104Z25
	L1002,	L1005,L1006,L3004-L3009	VTL1079			5,C6036,C6039,C6040,C6042	CKSRYF104Z25
	L3014,	L3015,L3018-L3022,L4002	VTL1079				
	19351	936,L943,L944	VTL1082			5,C6047,C6055,C7023,C7076	CKSRYF104Z25
	L1003,		VTL1084			5,C7097,C7201,C7202,C8006	CKSRYF104Z25
	L7017-		VTL1086			5,C8029–C8032,C8036,C8040 2,C8044,C8047–C8051	CKSRYF104Z25 CKSRYF104Z25
		L7004,L7006,L7008-L7010	VTL1124			7-C8061,C8070-C8072	CKSRYF104Z25
0454	OITO				00077	, 00070 00004 00000	01/00/15404705
CAPA	CITOR					7,C8078,C8081–C8083 5,C8086,C8089,C8091	CKSRYF104Z25 CKSRYF104Z25
	C901-		CCSQCH4R0C50			I,C8095,C8102,C8103	CKSRYF104Z25
		,C6041,C6046,C9026	CCSRCH102J50			,C8108,C8112,C8122,C8127	CKSRYF104Z25
	C9001 C3036		CCSRCH120J50 CCSRCH220J50			3-C9005,C9007,C9009-C9011	CKSRYF104Z25
	C9025		CCSRCH221J50		00040		01/00/5/04705
						3,C9015-C9017,C9019-C9024	
		-C5068	CCSRCH470J50			7,C9029–C9032,C9501–C9506 3–C9519,C9521–C9524	CKSRYF104Z25 CKSRYF104Z25
		,C1015,C8016,C8017,C812				6-C9535	CKSRYF104Z25
	C8129	C7107 C7112	CCSRCH471J50			5,C4006,C4015,C4016	CKSRYF105Z10
	C8123	,C7107,C7112 .C8131	CCSRCH5R0C50 CCSRCH750J50			, , ,	
		,				5,C4037,C7006–C7009,C7021	CKSRYF105Z10
		,C7093,C7095,C7105	CEV100M16			I,C7035-C7038,C7041	CKSRYF105Z10 CKSRYF105Z10
		,C2042,C7051,C8027,C804				I,C7045,C7048–C7050,C7052 I,C7059–C7064,C7067–C7074	
	C8121		CEV101M16			7,C7079–C7084,C7086–C7090	
		,C2025,C2031,C2032,C2044 ,C3025,C3026,C6043,C6044				,	
		, , , ,				2,C7094,C7099,C7102,C7103	CKSRYF105Z10
		,C8038,C8075,C8092,C8093				5,C7108–C7111,C7205,C8090	CKSRYF105Z10
		,C8097,C8109-C8111,C901			C6051	I,C9018	CKSRYF105Z10 CKSRYF474Z16
	C9525		CEV101M6R3			01 (20pF)	VCM1008
		,C1004,C1007,C2023 -C2039,C3001-C3003	CEV221M4 CEV221M4		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	(2001)	V 0.001000
		•		RESI	STORS	3	
		,C3040,C4001,C4002	CEV221M4			7,R4054,R4071,R5015,R5016	RAB4C0R0J
		-C4047,C4054,C5005 .C5008.C5022.C6004	CEV221M4 CEV221M4			3,R5024,R7081,R7089,R7115	RAB4C0R0J
		,C6034,C7003–C7005	CEV221M4 CEV221M4			9,R8082,R8095,R8103,R8121	RAB4C0R0J
		,C7034,C7039,C7065	CEV221M4			5,R8137,R8146–R8148	RAB4C0R0J
		, ,			K3137	′–R3142,R9017,R9018	RAB4C102J
		,C7085,C8033	CEV221M4			5,R9027,R9567	RAB4C102J
		,C8004,C8005,C8007,C8008				5-R1028,R1031,R1032,R1046	RAB4C103J
		,C8012-C8015,C8022 ,C7027,C7028,C7042,C7043	CEV330M25 3 CKSQYF225Z16),R1067,R1071,R1079	RAB4C103J
	C7056	, 5. 521, 5. 525, 5. 572, 5. 64	CKSQYF225Z16			5,R1096,R1115–R1122 3–R2035,R2040,R2060,R2064	RAB4C103J RAB4C103J
	C7078	.C7100	CKSQYF475Z10				
		,C5011,C5012,C5019,C502 [,]				I–R2078,R3001,R4086	RAB4C103J
		,C8039,C8076	CKSRYB102K50			5-R5109,R6029,R6034,R6039 3-R6045,R8047,R8048,R8118	RAB4C103J RAB4C103J
		,C2008,C2043,C3035,C501				3-R8135,R8143,R8144,R9009	RAB4C103J
	C5017	,C5020,C5041,C5044,C6048	CKSRYB103K50			6,R9065,R9066	RAB4C103J
	C6053	,C7055,C8069	CKSRYB103K50		R1033	3-R1036,R1039,R1041,R1044	RAB4C220J
					111000	, 11.300,11.1000,11.1041,11.1044	1.7.10-102200

Mark	No. Description P	art No.	Mark No. Description	Part No.
	R1059,R1061,R1063,R1065	RAB4C220J	R8090	RS1/16S1002F
	R1069,R1070,R1072,R1077	RAB4C220J	R8037	RS1/16S1003F
	R1080-R1084,R1089,R1091	RAB4C220J	R8091	RS1/16S1301F
	R1097-R1106,R2023,R2024	RAB4C220J	R7104,R7133	RS1/16S1501F
	R2037,R2038,R2041,R2044,R2045	RAB4C220J	R8080	RS1/16S1802F
	R2050,R2056,R2058,R2059,R2061	RAB4C220J	R8073,R8107	RS1/16S2201F
	R2063,R2069-R2073,R3010	RAB4C220J	R7103,R7132	RS1/16S2701F
	R3019,R3025,R3032	RAB4C220J	R7102,R7110,R7131	RS1/16S3300F
	R3036,R3037,R3045,R3052	RAB4C220J	R8093	RS1/16S3601F
	R3061,R3062,R3064,R3073	RAB4C220J	R1012,R7026,R7076	RS1/16S3900F
	R3079,R3080,R3082,R3083,R3093	RAB4C220J	R8074,R8116	RS1/16S5600F
	R3114-R3118,R3120-R3123	RAB4C220J	R9022	RS1/16S6341D
	R3125-R3128,R4007,R4008	RAB4C220J	VR7003-VR7005 (100Ω)	VCP1167
	R4010,R4011,R4015	RAB4C220J	VR7006,VR7007 (470Ω)	VCP1169
	R4025,R4028,R4029	RAB4C220J	Other Resistors	RS1/16S□□□J
	R4041-R4043,4046-R4051,R4053	RAB4C220J	OTHERS	
	R4056,R4059–R4062,R4066,R4068	RAB4C220J	OTHERS	
	R4070,R4072,R4074–R4076,R4078	RAB4C220J	X1001 (40MHz)	DSS1101
	R4080–R4082,R4084,R4085	RAB4C220J	X3002 (54.000MHz)	VSS1138
			X3001 (27.000MHz)	VSS1146
	R4089,R4090,R4093–R4095	RAB4C220J	X9001 (24.576MHz)	VSS1151
	D4007 D4404 D4406 D4444	DAD4C2201	X5001 (27.500MHz)	VSS1153
	R4097-R4104,R4106-R4111	RAB4C220J	710001 (271000mile)	
	R5006–R5009,R5057,R5071,R5078	RAB4C220J	CN8001 Connector	B10B-ZR-SM3
	R5084,R6002-R6007,R6021,R6022	RAB4C220J	CN2003 Connector	B14B-PH-SM3
	R6027,R6028,R6030,R6031,R6035	RAB4C220J		
	R6037,R6040,R6041,R6046,R6047	RAB4C220J	CN2002 Connector	B4B-ZR-SM3
			CN9001 Connector	B6B-PH-SM3
	R6057,R6059,R6061-R6064,R6086	RAB4C220J	CN6001 Connector	B6B-ZR-SM3
	R7042-R7044,R7056,R7061	RAB4C220J		
	R7067,R7068,R9004-R9008,R9010	RAB4C220J		NS-U005
	R9019,R9021,R9029,R9031,R9032	RAB4C220J		VDA1681
	R9037,R9046,R9057,R9058,R9064	RAB4C220J	CN1002 7P Connector	VKN1411
	N9037,N9040,N9037,N9030,N9004	KAB4C2203	CN2001 20P Connector	VKN1424
	D0067 D0070 D0500 D0540 D0547	DAD4C2201	CN7001 22P Connector	VKN1426
	R9067-R9072,R9509-R9512,R9517	RAB4C220J		
	R9520-R9522,R9528,R9529	RAB4C220J	CN3001 40P FFC	VKN1786
	R9536,R9537,R9540–R9542,R9545	RAB4C220J	KN1–KN6 Earth Metal Fitting	VNF1109
	R9556,R9557,R9563–R9566	RAB4C220J	MINI-MINO Latti Metal Fitting	VIVI 1109
	R9569-R9571,R9573,R9574	RAB4C220J		
	R9577-R9592	RAB4C220J	FL ASSY	
	R9033,R9034,R9041,R9042	RN1/16SC56R0D	FL ASST	
			CEMICONDUCTORS	
	R1023,R2098	RN1/16SE1001D	SEMICONDUCTORS	
	R8203,R8209	RN1/16SE1602D	IC1201	MSM9202-01
	R2097	RN1/16SE3001D	Q1601	2SB1238X
			Q1201,Q1501-Q1505	DTC124EUA
	R8204,R8213	RN1/16SE3302D	D1601,D1602	1SS355
	R1001,R1003,R1014,R1024,R1030	RS1/10S0R0J	D1505	LNG989CNBW
	R1048,R1051,R1066,R1078,R1085	RS1/10S0R0J	2.000	2.100000.1211
	R1107,R2001,R2006,R2007	RS1/10S0R0J	D1501,D1503,D1603	UDZ12B
	R2012-R2018,R2021,R2029-R2032	RS1/10S0R0J	D1506	UDZS6.2B
	R2036.R2083-R2085.R2094	RS1/10S0R0J		
	R3042,R3043,R3050,R3077,R3112	RS1/10S0R0J	COILS AND FILTERS	
	R45,R48,R49,R51	RS1/10S0R0J	L1601	LRCA100J
	R53,R56,R6008,R6012,R6013	RS1/10S0R0J	L1201	LRCA220J
	R6065,R6066,R6073,R6089,R7006	RS1/10S0R0J	LIZUI	LRCA2203
	K0005,K0000,K0075,K0009,K7000	K31/1030K03		
	R7020.R7021.R7023.R7037.R7041	RS1/10S0R0J	SWITCHES AND RELAYS	
	, - ,, , -		S1301-S1307	ASG7013
	R7047,R705,R7065,R707	RS1/10S0R0J		1.23.0.0
	R7085,R7086,R7111,R713,R7201	RS1/10S0R0J	0404017000	
	R724,R8001,R8012,R8015	RS1/10S0R0J	CAPACITORS	
	R8024,R8025,R8039,R8040,R8063	RS1/10S0R0J	C1206-C1208	CCSRCH101J50
			C1209	CCSRCH390J50
	R8168,R8205,R9011,R9073,R9507	RS1/10S0R0J	C1210,C1603	CEAT100M50
	R9527,R9568	RS1/10S0R0J		
	R5067	RS1/10S100J	C1203,C1212	CEAT101M10
	R2022,R2026,R2027	RS1/10S100J	C1605	CEAT101M16
	R5066	RS1/10S150J	04400	05100041440
	1.0000		C1402	CEJQ221M10
	R7099	RS1/10S220J	C1301,C1403,C1501,C1606	CKSRYB103K50
			C1211,C1601,C1602	CKSRYF103Z50
	R7022,R7075,R8094	RS1/16S1001F	C1205,C1213	CKSRYF104Z25
			C1204	CKSRYF105Z10

DVR-7000

S1/16S□□□J IR-FJ 'R-FJ 'B-PH-K P1U28X _EM20S-1 AW1067 EB1125 NF1087		Q311 D134,D	1910 1122,Q131,Q501 220,D311,D424 122,D252,D453	VZF1112 VZF1113 VZF1114 VZF1115 10ELS2 1SS270A MTZJ39D UK1V26
IR-FJ 'R-FJ 7B-PH-K P1U28X LEM20S-1 AW1067 EB1125		Q111,Q Q311 D134,D D112,D D211 D103 D212	220,D311,D424	VZF1114 VZF1115 10ELS2 1SS270A MTZJ39D UK1V26
IR-FJ 'R-FJ 7B-PH-K P1U28X LEM20S-1 AW1067 EB1125		Q311 D134,D D112,D D211 D103 D212	220,D311,D424	VZF1115 10ELS2 1SS270A MTZJ39D UK1V26
'R-FJ 'B-PH-K P1U28X LEM20S-1 AW1067 EB1125		D134,D D112,D D211 D103 D212		10ELS2 1SS270A MTZJ39D UK1V26
'R-FJ 'B-PH-K P1U28X LEM20S-1 AW1067 EB1125		D112,D D211 D103 D212		1SS270A MTZJ39D UK1V26
'R-FJ 'B-PH-K P1U28X LEM20S-1 AW1067 EB1125		D211 D103 D212	122,D252,D453	MTZJ39D UK1V26
7B-PH-K P1U28X LEM20S-1 AW1067 EB1125		D211 D103 D212	122,0202,0400	MTZJ39D UK1V26
P1U28X LEM20S-1 AW1067 EB1125		D103 D212		UK1V26
LEM20S-1 AW1067 EB1125		D212		
AW1067 EB1125				VZF1045
EB1125				VZF1051
EB1125				
		D210,D	410	VZF1053
		D612		VZF1057
		D101		VZF1063
		D901		VZF1075
		D701		VZF1081
		D451 D	452	VZF1083
				VZF1083
TC124EUA				VZF1088
		,	· · ·	VZF1100
0.0.0			123	VZF1105
		D000 =	00.4	\/ 7 =
SG7013				VZF1118
				VZF1119
J. 1. 00 =				VZF1117 r VZF1116
		. 0.0.	1 0 100,1 000 1 1 110.0 00apioi	v <u>2</u> o
KSRYB103K50	RESIS	STORS		
	\triangle	R410	Fusible Resistor(10 Ω)	VZC1063
		R212	Fusible Resistor(47Ω)	VZC1065
S1/16S□□□J				
	OTHE	RS		
	\triangle	P221,P	226 Fuse(1A)	VEK1041
D EI		P610		VEK1042
F-F3	\triangle	P252,P		VEK1048
	$\overline{\triangle}$			VEK1056
	\triangle	P815	Fuse (3.5A)	VEK1073
	A	EI 1404	Fuco (2.15A)	VEK1044
	<u> </u>	10101	Fuse (3.13A)	v ⊑K 1044
SG7013				
KSRYB103K50				
NOINTE TUSINOU				
24/460000				
51/165UUUJ				
וחו דו				
IPL-FJ				
	S1/16S□□□J ′P–FJ	LR-343VC SG7013 SX1002 KSRYB103K50 RESIS A S1/16S□□□J OTHE A A A A SG7013 KSRYB103K50 S1/16S□□□J	D251,D D510,D D510,D D127 D110,D D222,D D421-D TH451 PC101- KSRYB103K50 RESISTORS △ R410 R212 S1/16S□□□J OTHERS △ P221,P △ P610 △ P252,P △ P271,P △ P815 △ FU101 SG7013 KSRYB103K50 S1/16S□□□J	D127 D110,D123 D222,D224 D421-D423 TH451 Thyristor(3P4J) PC101-PC103,PC501 Photo Couple CSRYB103K50 RESISTORS Δ R410 Fusible Resistor(10Ω) R212 Fusible Resistor(47Ω) S1/16S□□□J OTHERS Δ P221,P226 Fuse(1A) Δ P610 Fuse (0.75A) Δ P252,P611 Fuse (1.5A) Δ P271,P701,P915 Fuse (2.5A) Δ P815 Fuse (3.5A) Δ FU101 Fuse (3.15A) SG7013 CSRYB103K50 S1/16S□□□J

POWER SUPPLY ASSY

SEMICONDUCTORS

IC271,IC301	VZF1089
IC801,IC910	VZF1107
Q252,Q272,Q410,Q911	2SC1740
Q312	2SC2655
Q313	DTC114ES
Q314	DTC143ES
Q120	VZF1101
Q110	VZF1108
Q211	VZF1109
Q221	VZF1110
Q251	VZF1111
	IC801,IC910 Q252,Q272,Q410,Q911 Q312 Q313 Q314 Q120 Q110 Q211 Q221

■ (REFERENCE) RECORDER DRIVE MAIN ASSY CONTRAST TABLE

This service manual does not include ASSY PARTS LIST of the RW RECODER SECTION. But as a reference, the CONTRAST TABLE between the RECORDER DRIVE MAIN ASSY of DVR-7000 and DVR-A03 are listed as following.

DWX2148 and DWX2147 are constructed the same except for the following:

		Part No.		
Mark	Symbol and Description	(DVR-A03) DWX2147	(DVR-7000) DWX2148	Remarks
	IC100 IC111 IC110 IC113 IC303,305	Not used UPD72153GM-UEU EL6257CU PCM1719E TC4W53FU	TC7WH08FU UPD72153AGM-UEU Not used Not used Not used	*
	IC306 IC501 IC502 IC503 Q102,Q103	M37902FGCHP SM8706AV K4E151612D-TL50 RL5E839 HN1B04FU	M37911FGCHP SM8706BV Not used Not used Not used	
	Q106 Q107-Q110,Q401 D101-D104 L105-L108 L1000,L1001	DTA114EK 2SD2114K 1SS355 PTL1014 DTL1087	Not used Not used Not used Not used Not used	
	L1011,L1012,L1100,L1108-L1110 C95 C100 C131 C154,C163,C175	Not used Not used Not used CKSRYB102K50 CKSRYF104Z25	VTL1079 CKSRYB105K6R3 CKSRYF104Z25 CCSRCH221J50 CKSRYB105K6R3	* * *
	C138,C146 C169,C172 C93,C94 C102,C105 C104,C197,C306,C307,C502-C507,C515	CKSRYF105Z10 CCSRCH221J50 CKSRYB102K50 CKSRYB104K16 CKSRYF104Z25	CKSRYB105K6R3 Not used Not used Not used Not used	
	C516,C519,C522,C524-C532,C1102 C1108,C1112,C1113,C1123,C1124 C170 C193 C179-C183	CKSRYF104Z25 CKSRYF104Z25 CKSQYF225Z16 CKSRYB103K50 CKSRYB104K16	Not used Not used Not used CKSRYB104K16 CCSRCH471J50	
	C518 C521 C517 C520 C501	CKSRYB472K50 CKSRYB562K50 CKSRYB393K16 CKSRYB473K16 CKSQYF225Z16	Not used Not used Not used Not used Not used	
	C523 C807 C1103,C1109 C1114,C1115,C1122 C1137,C1138(4.7mF/16V)	CKSQYF225Z16 CKSRYF104Z25 CEV100M16 CEV470M6R3 DCH1142	Not used CKSRYB104K16 Not used Not used Not used	
	C1110,C1111 C1131 C1116,C1117 C1024,C1025 R98,R99	CKSRYB122K50 CKSRYF103Z50 CKSRYF224Z16 Not used Not used	Not used Not used Not used CKSRYB102K50 RS1/10S0R0J	* *
	R100,R341,R342,R414,R1120,R1122 R1123,R1124,R1126,R1128 R109 R156 R109	Not used Not used RS1/16S151J RS1/16S680J RS1/16S151J	RS1/16S0R0J RS1/16S0R0J RS1/16S221J RS1/16S220J RS1/16S221J	*

		Part	No.		
Mark	Symbol and Description	(DVR-A03) DWX2147	(DVR-7000) DWX2148	Remarks	
	R188	RS1/16S222J	RS1/16S0R0J		
	R150	RAB4C103J	Not used		
	R194	RS1/16S180J	Not used		
	R104,R105,R119,R189,R195,R196	RS1/16S102J	Not used		
	R158,R164,R174,R177,R182,R197,R1102	RS1/16S222J	Not used		
	R187	RS1/16S392J	Not used		
	R185,R193,R520	RS1/16S103J	Not used		
	R106,R110	RS1/16S473J	Not used		
	R180,R186	RS1/16S104J	Not used		
	R232,R519,R530,R1121,R1125,R1127	RS1/16S0R0J	Not used		
	R531	Not used	RS1/16S103J	*	
	R509,R510	RS1/16S220J	Not used		
	R523,R524	RS1/16S470J	Not used		
	R518	RS1/16S510J	Not used		
	R521,R522,R532,R1100,R1107-R1110	RS1/16S101J	Not used		
	R516	RS1/16S431J	Not used		
	R514	RS1/16S821J	Not used		
	R517	RS1/16S302J	Not used		
	R515	RS1/16S432J	Not used		
	R511,R512	RAB4C330J	Not used		
	R923	RS1/16S391J	RS1/16S471J		
	R1013	Not used	RS1/16S471J	*	
	R1014	Not used	RS1/16S101J	*	
	R1101	RS1/16S180J	Not used		
	R1114	RS1/16S511J	Not used		
	R1112	RS1/16S151J	RS1/16S471J		
	R1113	RS1/16S333J	RS1/16S0R0J		
	R1105	RS1/16S105J	Not used		
	R1129-R1132	RS1/16S0R0J	RS1/16S221J		
	VR105 (10KΩ)	DCP1080	Not used		
	CN403 (Connector)	Not used	S6B-PH-SM3	*	
	CN405 (Connector 6P)	Not used	DKN1224	*	
	CN406 (Connector))	Not used	S4B-ZR-SM3A	*	
	CN407 (Connector 6P)	Not used	S6B-ZR-SM3A	*	
	CN409 (40P Flexible Connector)	Not used	DKN1230	*	
	JA101(Jack)	DKN1123	Not used		
	CN401 (LK Connector)	LK-44104H-S1D1Z-2	Not used		
	CN402 (ZH Connector 2P)	B2B-ZR-SM3	Not used		
	CN408 (2P Digital Out Connector)	DKN1176	Not used		

^{* :} Additional parts for DWX2148

6. ADJUSTMENT

6.1 3D Y/C ASSY ADJUSTMENT

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
1	Y/C input level adjustment (Input system adjustment)	VR3301	TUMJ ASSY CN3001 Pin10(SEL Y)	1 / UUVD-D T AUIDV	Input a white 100%(1.0Vp-p) signal into Input 1 (composite). (75 Ω termination)

6.2 TUMJ ASSY ADJUSTMENT

6.2.1 TUMJ ASSY ADJUSTMENT TABLE

Note: Use disc: [DVD test disc GGV1025]

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
1	Video level adjustment of terrestrial wave (Input system adjustment)	VR4101	TUMJ ASSY CN3001 Pin10(SEL Y)	2.00Vp-p ± 80mV	Input a signal of fv=EIA color-bar $60dB\mu V$ to terrestrial wave input. /through output.
2	Audio multiplex ATT adjustment (Input system adjustment) Refer to 6.2.2.	IC4601 (IIC bus adj.)	Audio ouput (R) (Rear panel)	310mVrms± 9.3mV	Input a signal of Mono 1kHz/100% modulation to terrestrial wave input. /through output. (Rec level = \pm 0) Note 2
3	Audio multiplex WIDE BAND adjustment (Input system adjustment) Refer to 6.2.2.	IC4601 (IIC bus adj.)	Audio ouput (R) (Rear panel)	Best point of separation ≥30dB Note 1	Input a signal of Stereo 300Hz/30% modulation (NR-ON) to terrestrial wave input. /through output Note 2
4	Audio multiplex SPECTRAL adjustment (Input system adjustment) Refer to 6.2.2.	IC4601 (IIC bus adj.)	Audio ouput (R) (Rear panel)	Best point of separation ≥25dB Note 1	Input a signal of Stereo 3kHz/30% modulation (NR-ON) to terrestrial wave input. /through output Note 2
5	Y level adjustment of component system (Output system adjustment)	VR1311	Component ouput (Y) (75Ω terminate)	1.0Vp-p ± 40mV	100% white data playback (DVD-REF-A1 T2-C5,etc)
6	PB level adjustment of component system (Output system adjustment)	VR1313	Component ouput (PB) (75Ω terminate)	714mVp-p ± 28mV	100% white data playback (DVD-REF-A1 T2-C19,etc)
7	PR level adjustment of component system (Output system adjustment)	VR1312	Component ouput (PR) (75Ω terminate)	714mVp-p ± 28mV	100% white data playback (DVD-REF-A1 T2-C19,etc)

Note 1: The values for channel separation is defined as those having passed through the following filters:

100Hz - 10kHz : +0/-0.5dB 15.75kHz - 100kHz : -40dB or more

Note 2: The audio multiplex adjustment No.2 – No.4 is done under the debugging mode. Refer to 6.2.2 about the details.

81

6.2.2 AUDIO DEMULTIPLEX ADJUSTMENT MODE

This section describes how to set the each parameter of US Audio Multiplex Decoder IC (CXA2094Q) on the TUMJ ASSY and memorize the data on the EEPROM in the TUMJ ASSY.

The adjustable parameters and setting data are following:

ATT 00 ~ 15
 Wideband 00 ~ 63
 Spectral 00 ~ 63

■ How to Setting

■ Use Service Remote Control Unit [GGF1067]

How to Enter the Audio Demultiplex Adjustment Mode

Press the [ESC] and [P.RUN] buttons sequentially.

Then the screen turns to Audio Demultiplex Adjustment Mode, and displays the following screen.

How to Change the Parameter

① ATT
 ② Wideband
 Increase or decrease the setting data by [SPEED+] or [SPEED-]
 ② Wideband
 Increase or decrease the setting data by [SCAN>>] or [SCAN<<]

③ Spectral Increase or decrease the setting data by [STILL STEP|>] or [STILL STEP<|]

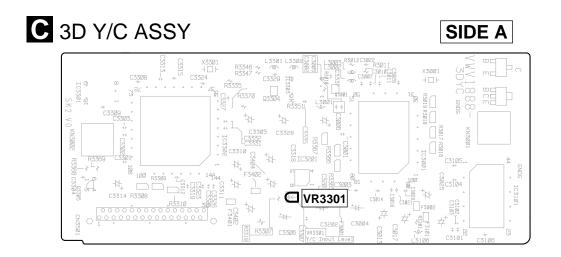
The level display(bar-graph) and setting data are displayed at the right side of each item.

How to Memorize the Setting Data

Press the **[PLAY]** key of GGF1067 to memorize the data on the EEPROM in the TUMJ ASSY after setting each parameter. (The data is not erased even if the AC plug is disconnected from the outlet.)

How to Exit the Audio Demultiplex Adjustment Mode

Press the **[ESC]** key of GGF1067 to exit the Audio Demultiplex Adjustment Mode. Then the mode screen disappears.



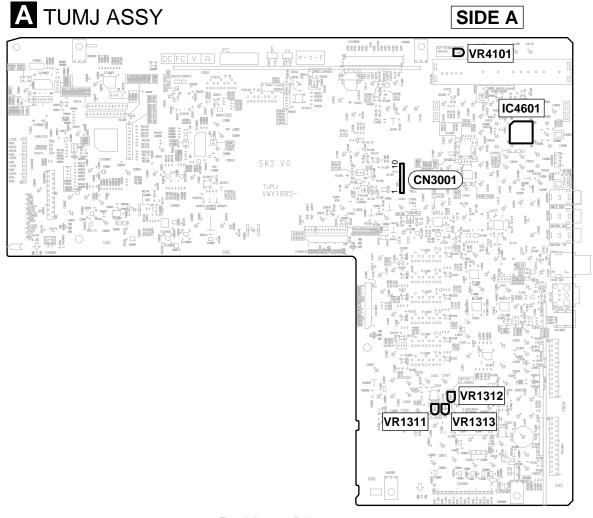


Fig1. Adjustment Point

6.3 MAIN ASSY ADJUSTMENT

Note: Use disc: [DVD test disc GGV1025]

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
1	Master clock free-running adjustment (Clock system adjustment)	VC3001	MAIN ASSY IC4007 Pin54 (CLKO) (M65774AFP)	27.000000MHZ ± 130Hz	No input signal or during test disc play-back
2	Y level adjustment of CVBS system (Output system adjustment)	VR7006	Y output of S terminal (75Ω termination)	1.00Vp-p ± 40mV	Playback the DVD test disc(100%white). Terminate the Y output of S terminal with 75Ω and adjust so that the level of between sync tip and white peak becomes 1.0Vp-p.
3	C level adjustment of CVBS system (Output system adjustment)	VR7007	C output of S terminal (75Ω termination)	286mVp-p ± 11mV	Playback the DVD test disc(100%color- bar). Terminate the C output of S terminal with 75Ω and adjust so that the amplitude of color burst becomes 286mVp-p.
4	Y level adjustment of component system (Output system adjustment)	VR7003	MAIN ASSY CN7001 Pin11 (Y Out)	800mVp-p ± 24mV	Playback the DVD test disc(100%white). At the pin 11 of CN7001 in the MAIN ASSY, adjust so that the level of between sync tip and white peak becomes 0.8Vp-p.
5	PB level adjustment of component system (Output system adjustment)	VR7004	MAIN ASSY CN7001 Pin13 (PB Out)	760mVp-p ± 22mV	Playback the DVD test disc(100%color-bar). At the pin 13 of CN7001 in the MAIN ASSY, adjust so that the level of between bottom and top becomes 0.76Vp-p in the 100% color-bar screen.
6	PR level adjustment of component system (Output system adjustment)	VR7005	MAIN ASSY CN7001 Pin15 (PR Out)	760mVp-p ± 22mV	Playback the DVD test disc(100%color-bar). At the pin 15 of CN7001 in the MAIN ASSY, adjust so that the level of between bottom and top becomes 0.76Vp-p in the 100% color-bar screen.

E MAIN ASSY



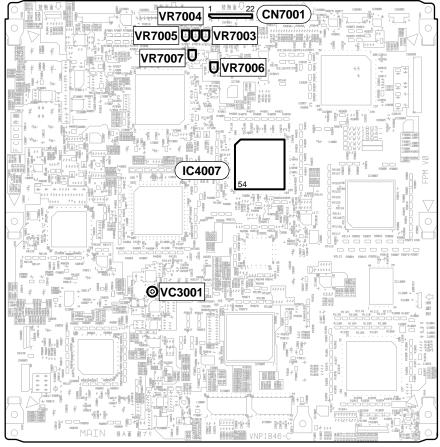


Fig.2 Adjustment Point

7. GENERAL INFORMATION

7.1 DIAGNOSIS

7.1.1 MODEL TYPE AND REGION SETTING

■ Setting the Model type and Region No. for DVD Recorder

For the DVD recorder DVR-7000/KU/CA and /LB type, it is necessary to set the region No. [1 or 3] on the FLASH ROM in the MAIN ASSY and the model type [KU or LB] on the EEPROM in the TUMJ ASSY. So when the MAIN ASSY or TUMJ ASSY is renewed, "The Model type and Region setting mode screen" is displayed automatically.

Note: If the region No. is once set, it is unable to rewrite it. When it is necessary to change the region No., renew the MAIN ASSY. And it is able to rewrite the once set model type on the EEPROM in the TUMJ ASSY only when the MAIN ASSY is renewed and setting the new region No. on the FLASH ROM.

How to set the Model type and Region No.

- 1. Turn the power on.
- The setting request screen is displayed when the model type and region No. is not set. At this time FL displays " MODE SETTING".

[Recorder's Model and Region Setting]
Please pick out any one of the following.

Button No. Model Region
[1 : KU_MODEL<North America> Region 1]
[2 : LB_MODEL <Taiwan> Region 3]

- 3. Enter the data according to the mode menu by the service remote control unit.
- 4. The recorder restarts automatically.
- Set the shipping position. (stop + power off)
 But it is omitted when making the Down Load of the system μ-com is done after this.
- 6. Turn off the power, then turn on the power again.

● When the FL displays "MODEL MISMATCH" after connecting the AC plug to the outlet.

It displays, connecting the AC plug to the outlet when the setting is mismatched between the software setting of the model type data on the EEPROM and the μ -com hardware pin setting of the model type in the TUMJ ASSY. At this time, it is unable to turn on the power.

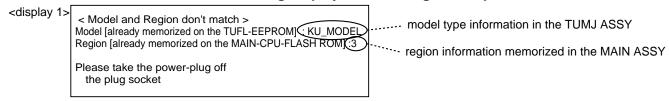
It is considered the TUMJ PCB board fault (model type hardware pin setting fault).

Note : [Tuner control μ -com hardware pin setting of the model type]

Pin 76=Region 1, Pin 77=Region 2, Pin 98=Region 3

Pull up the correspond pin to $Vcc(V+3_3M)$ and pull down other setting pins to GND by $10k\Omega$ resistor.

When the screen shows the following display after turning on the power

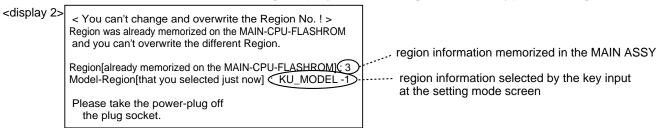


It displays, exchanging the MAIN ASSY or TUMJ ASSY, etc when the combination of model type and region No. already set is mismatched.

After this, it is unable to operate any functions.

Match the combination between the model type and region No. setting, or renew the ASSY and set the data newly.

When the screen shows the following display after setting the Model type and Region No.



It displays, renewing TUMJ ASSY,etc when setting the different model type from the region No. already set in the FLASH ROM in the MAIN ASSY.

Match the combination between the model type and region No. setting, or renew the MAIN ASSY and set the data newly.

7.1.2 CPRM ID NUMBER AND ID DATA SETTING

■ Use ID DATA DISC [GGV1065] and Service Remote Control Unit [GGF1067]

■ Entering the ID Number and ID Data for DVD Recorder

For the DVD recorder, it is necessary with the recoding/playback of DVD–RW disc to set an individual number (ID number) and ID data to each recorder. If the number and data are not set correctly with the following procedure, operations in the future may not be guaranteed. You will find the ID number to be set on the ID label on the rear panel.

Important: If no ID label is found on the rear panel, write down the specified ID number by checking it according to "How to confirm the ID number" shown below.

The Input is Necessary When:

- " CPRM ERR" is displayed on the FL display immediately after the power is turned on or in Stop mode.
- · When the MAIN ASSY, RECORDER DRIVE MAIN, CPRM LSI or the FLASH ROM is exchanged.

Note

Be sure to enter the ID number in Stop mode.

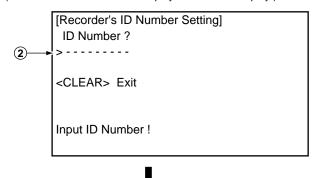
Use the service remote control (GGF1067) for operations. Only opening/closing of the tray are performed from the player. The ID data disc is swept out automatically after the recorder have read the data from it.

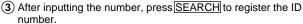
How to Input the ID Number and ID Data

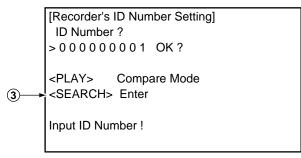
1 To enter the input mode, press ESC + STEREO in a status with no ID number set, such as after FLASH-ROM downloading.



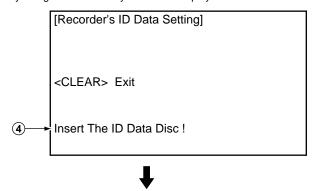
② As number input is enabled when the unit enters the input mode, input the 9-digit ID number. (The entered number is also displayed on the FL display.)



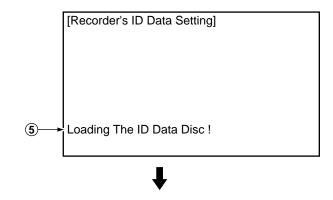




(4) When the ID number has been registered, the unit enters the ID data input mode. (The FL display indicates "INSERT ID DATA.") In this condition, place the ID data disc on the tray and close the tray using the CLOSE key "■/▲" on the player.



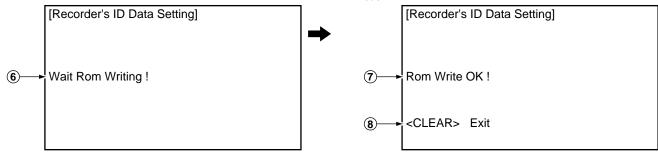
(5) While the data are being read, the message shown in the figure at left is displayed on the screen. (The FL display indicates "LOAD ID DATA.")





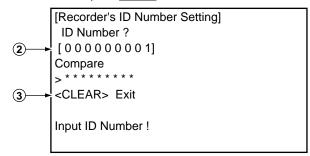
- (6) When the ID data have been read, the data are written to the FLASH-ROM.
 - (The FL display indicates "WRITE ID DATA.")

- (7) When the ID data have been written to the FLASH-ROM, the message "Rom Write OK" is displayed on the screen. (The FL display indicates "ID DATA OK.")
- (8) After confirming this message, press CLEAR to exit the input mode.



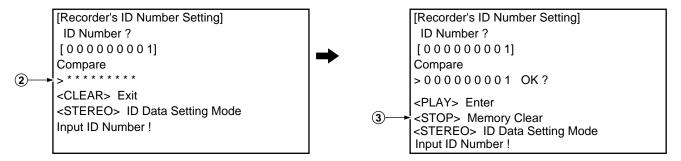
How to Confirm the ID Number

- 1 Press ESC + STEREO with an ID number set, and the unit enters the ID number confirmation mode.
- 2 The set ID number is displayed on the screen (and on the FL display), permitting you to confirm it.
- (3) To exit this mode, press CLEAR.



How to Clear the ID Number

- 1 Press ESC + STEREO with an ID number set, and the unit enters the ID number confirmation mode.
- 2 Input the same number as the ID number you have set.
- (3) After inputting the number, press STOP. Only when the entered number matches the set ID number, the ID number is cleared and the unit exits this mode. If the numbers do not match, you must return to step 2. (STOP is not accepted until 9 digits are entered.)



7.1.3 DEBUGGING MENU

For operation, use the GGF1067 remote control unit for service.

The Debug menu is a main menu from which to select any of 11 mode menus, classified by rough category, such as recording system and VR playback system. The mode menus also have subscreens if there are many items.

The Debug menu during playback of a DVD-V (including video mode), CD, or VCD is almost the same as that of the DV-737 (see Mode Menu 10).

• How to Enter the Debug Menu : Press [ESC] + [DISP] keys in order while no GUI is displayed.

How to Exit the Debug Menu : Press the [ESC] key.
 How to Advance the Mode Menu : Press the [DISP] key.

• How to Advance the Subscreen in a Mode Menu : Press the [DIG/ANA] key.

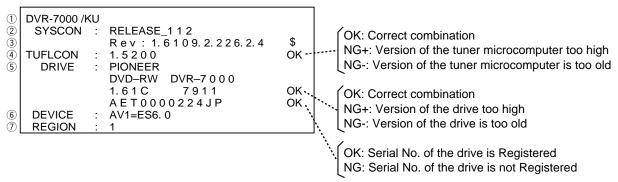
Note 1: If you press the [DISP] key on the final mode menu, the display will return to Mode Menu 1.

Note 2 : Pressing the [DIG/ANA] key repeatedly will change the subscreens within the same mode cyclically. To change mode menus, press the [DISP] key.

■ Description of Each Mode

1. Mode Menu 1 [Version information, etc.]

Subscreen 1



- ① Model name/destination
- 2 Version of the recorder software
- 3 Revision No. of the system control computer software
- 4 Version No. of the tuner microcomputer, result of confirmation on combination between the tuner microcomputer and the system control computer
- (5) Information on the built-in drive (Name of the manufacturer, model name of unit into which the drive is built, version No., CPU model name, serial No., result of confirmation of combination with the system control computer*2
- 6 Version No. of AV1
- ? Region No.

Subscreen 2

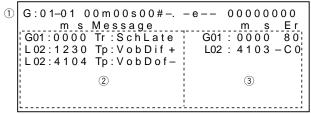
1	ERR RATE : x. x x E-x /

Error rate during playback in VR mode (Averaging value for last 10VOBUs),
 Display the rotation ratio of the drive (/: Normal speed, No display: Double speed)
 Note: Be sure to start playback after displaying this screen.

2. Mode Menu 2 [VR playback (related to decoding), debug display]

- Subscreen 1 (This menu is for design use.)
- Subscreen 2

Error history of VR playback



1 Information on location of the display

Original (G)/Play List (L), title, chapter [X:XX-XX], time of the display (min, sec, frame) [XXmXXsXX], busy mark of the virtual mechanical control computer [#], error rate of the transfer data [X.XeXX], playback logical address (ID) [XXXXXXXX]

2 Error Message history

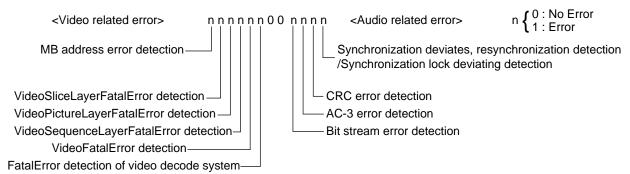
Original (G)/Play List (L), title, time of occurrence (min, sec) [XXX:XXXX], playback-related error history for the last 8 errors [XX:XXXXXXX]

Note:

- For details on error information, see Table 7.1 "Description of VR playback-related errors," page 92.
- When an error occurs here, expect that there is a problem in data reading from the disc. (The possibility that there is a problem in the drive side is high.)

3 AV1 error status history

Original (G)/Play List (L), title, time of occurrence (min, sec) [XXX:XXXX], AV1 error status [XXX]. (The details are as follows.)



Note

- When there is not an error of ②, and an error of ③ occurs here, there is a problem in the AV side. (The possibility that there is a problem in AV1 tip or DVxcel is high.)
- When there is not an error of ② and ③ together, the screen is frozen and a sound breaks off, the possibility that a source itself is such a thing is high, and it is most of not to be trouble.
- Subscreen 3 (This menu is for design use.)

3. Mode Menu 3 [iLink-related debug display]

Subscreen 1

```
[Recorder] GUID: XXXXXXXXXXXXXX
  BGC: XXXX
            TN:XX
                  DN:XX
                         CA:X ER:X
            CD:XX CG:XX OC:X IC:X
3
  CT:XXXX
(4)
  PE:XXXX
1
            GUID: XXXXXXXXXXXXXX
(5)
  VN:XXXXXXXXXX MN:XXXXXXXXXXXX
  PW:XX TRM:XX
                 TRS:XX
```

- ① GUID Show the Global Unique ID (EUI-64)
- 2 BGC Show the bass reset processing number of times
 - TN Show the existing i.LINK equipment total number on the same bass. (Include recorder)
 - DN Show the existing DV equipment total number on the same bass
 - CA Show whether there are data in the stream buffer of 1394 LINK chip [Y/N]
 - ER Show whether an error occurred in the driver section.
- 3 CT Show format of the connection that recorder organized [BROAD/PTOP]
 - CD Show format of the connection that recorder organized [IN/OUT]
 - CG Show whether a broadcast-out connection was taken by other equipment
 - OC Show number of a connection organized to Output Plug
 - IC Show number of a connection organized to Input Plug
- PE Show number of the packet error that detected by 1394 LINK chip
- 5 VN Show Vendor Name of DV equipment
 - MN Show Model Name of DV equipment (There is the case that cannot get by equipment.)
- 6 PW, TRM, TRS

Show the various state that got from DV equipment (Do not get it except DV input selection time.)

4. Mode Menu 4 [DVxcel-related debug display]

Subscreen 1, Subscreen 2

(These menus are for design use.)

5. Mode Menu 5 [Mode-related debug display]

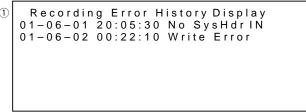
● Subscreen 1-7

(These menus are for design use.)

6. Mode Menu 6 [VR recording-related debug display]

- Subscreen 1-3 (These menus are for design use.)
- Subscreen 4

Error history of VR recording



① Recording-related error history of the last 9 times × 2 pictures

[occurrence time (yr-mo-day hr:min:sec), error information (in simplified description)]

Notes:

- •The two error-history pages can be switched by pressing the [SPEED +] or [SPEED -] keys.
- •For details on error information, see Table 7.2 "Description of VR recording-related errors," page 93.
- Subscreen 5− 11 (These menus are for design use.)

7. Mode Menu 7 [VR playback-related debug information]

Subscreen 1−3

```
G01 - 01
                          00:20'13"00
      Ep01
Vrplay 000 Flgw
                    Rev: 1, 55, 8, 3
Err
        Flgw
Read
                          Flg:0000a
DIRd-Slep DMA-Dnnl
                          Flg: 00801
Spd: 01-000
                 8. 25E -5/
                              Enp:8
Lsn:057a00 Err: 6.93E-5 Tn:0053n
                 8.41E - 5
    057a80
                              0054
    057b80
                  6.27E - 5/
                              0053
                  6.60E-5
    057ba0
                              0054
```

1) Display position information

Original (G)/Play List (L), title No., cell No. [XXX-XX], chapter (entry point) [EpXX], time of the display (min, sec, frame) [XX:XX'XX"XX]

2 Error rate information (four histories)

Logical address [Lsn:XXXXXX]

(Inner periphery: 0-100000h, Outer periphery: 180000-230000h)

Error rate [Err:X.XXE-X]

Rotation ratio display of the drive (/: Normal speed, No display: Double speed)

Command execution time ([Tn: XXXXns]

(Normally, double speed playback is 60ms degree in the internal periphery and it is 50ms degree in the outer periphery.)

- * When normal playback and command execution time are long, problem occurs in performance of readout from the disc. (Crack and dirt of the disc, and pickup of the drive is dirty, etc..)
- Subscreen 2-4 (These menus are for design use.)

8. Mode Menu 8 [ATA/ATAPI-related debug display]

- Subscreen 1-2 (These menus are for design use.)
- Subscreen 3

```
ATA/ATAPI
             WRITER & Vmecha & FAN
  powerON
             00 00 00 0000 0000000
  00000106
                00 00
                       0000 0000000
             0 1
                       0000
  LaserON
                 00 00
                             0000000
             0.2
  00000142
             03
                 0 0
                    0 0
                       0000
                             000000
  Recording
             04
                 00 00
                       0000 0000000
  000000A
             0.5
                00 00
                       0000 0000000
4
  FAN:OFF
                 0 0
                             000000
             06
                    00
                       0000
  TEMP: CB
(5)
             0.7
                 00 00
                       0000 0000000
  00000050 - 00000348
```

- 1 Power ON time of the drive (HEX display) [XXXXXXXXhour]
- ② Laser ON time except during record (playback) (HEX display) [XXXXXXXXhour]
- 3 Recording time (HEX display) [XXXXXXXXhour]
- 4 Active state of the Fan for drive (ON/OFF)
- 5 Temperature in the drive [XX] (CB: 45°C, One count: Convert it with ±1.6°C)
- - * 1)-3 data is stored even if power turned off.

9. Mode Menu 9 [GUI-related debug display]

● Subscreen 1–2 (These menus are for design use.)

10. Mode Menu 10 [DVD VIDEO playback-related debug display]

● Subscreen 1– 10 (These menus are for design use.)

These subscreens have been exported from the debugging displays of the DV-737. For details on display content, refer to the service manual for DV-737 (Order No. RRV2320).

11. Mode Menu 11 [DVD VIDEO key processing history display]

• Subscreen 1 (This menu is for design use.)

Error Message	Description
Tr : NullBlk	Transfer task: NULL at the top block (Detecting NG stream made at the DVR-1000 series and starting protection process.)
Tr : ReadErr	Transfer task: ATA read error
Tr : SchLate	Transfer task: ATA search late
Tr : SemTOvr	Transfer task: Timeout for gaining semaphore (no synchronization with the display)
Tr : NaviErr	Transfer task: Inconsistency between NAVI (navigator) of management data and actual NAVI
Tr : OrderEr	Transfer task: Inconsistent order
Mn : Av1Hang	Main task: Detects hang-up of AV decoder and starts recovery
ERR_RCV!	TPP task: Detects hang-up of AV decoder and starts recovery
Tp : VobDif+	TPP task: The decoder STC advances by 1 VOBU hour.
Tp : VobDif-	TPP task: The STC of the management information advances
Tp : midNULL	TPP task: The management information pointer designated was NULL.
Tp : ScanNg	TPP task: Failure to set the TPP memory when scanning was canceled.
Tp : RStepEr	TPP task: Although the reverse step had failed, the operation was forcibly terminated because the top cell was located.
Tp:tppErr	TPP task: Inconsistency occurred.
Rv : 1stTOvr	Reverse playback task: Timeout for waiting for interruption to the top VOBU immediately after starting decoding
Rv : OpnTOvr	Reverse playback task: Timeout for waiting for B-picture of the open GOP immediately after starting decoding
Rv : OplTOvr	Reverse playback task: Timeout for waiting for I-picture of the open GOP immediately after starting decoding
Rv : LnkTOvr	Reverse playback task: Timeout for waiting for link
Rv : LnkFail	Reverse playback task: Starts compensation by detecting link failure
Rv : R2FTOvr	Reverse playback task: Starts retrial after detecting timeout from reverse pause to forward pause
Rv : TopVbEr	Reverse playback task: Forced termination because of a possible error of the top data during reverse normal playback
Rv : OrderEr	Reverse playback task: Inconsistent order
Av : B/CTOvr	AV1: Buffer-clear timeout
Av : StrmOvr	AV1: Timeout for waiting for stream ready
Av : TpmTOvr	AV1: Timeout for TP mode change
Av : SpmTOvr	AV1: Timeout for a step command
CC_OS_ERR	Closed caption task: OS error
DAC_NG	Number of retrial for DAC setting is over.
DAC_Error	Failure to DAC setting

Table 7.1 Description of VR playback-related errors

[REFERENCE]

STC=System Time Clock , VOBU=Video Object Unit , GOP=Group Of Picture , B-picture=Bidirectionally predictive-picture |
I-picture=Intra-picture, P-picture=Predictive-pictute, TP mode change=AV1 term (Trick Play mode change)

Error Message	Description	Error Message	Description
Non Err	Normal	No Video	No video input (not locked)
DRAM NG	Abnormality in access to the DRAM for work	Invalid Param	Invalid parameter
SRAM NG	Abnormality in access to the backup SRAM for work	Protect Src	Source to be recorded is write-protected.
CPRM IC NG	Inappropriate CPRM IC	Now Busy	In the process of the emergency processing
Drive Destroy	The drive was destroyed.	Invalid Disc	The disc cannot be recognized.
MKB REVOKED	Error in gaining data	Invalid UDF	Invalid UDF content
BK BATT Down	Backup RAM data has been erased.	Invalid VMG	Invalid VMG content
BK FSYS Dirty	Backup RAM data has not been written on the file system.	Invalid TMVMG	Invalid TMP_VMGI content
Stream NG	Inappropriate input stream data	Unmatch Stamp	Impossible to modify because of unmatched time stamps
Stm Start NG	Failure to start encoding (reasons not clear)	Virgin DISC	Blank disc
Excel Hang	Dvexcel NG was announced.	Fail Repair	Repair failed.
No SysHdr IN	System packet is not input periodically.	ReadOnly DISC	Because part of data is invalid, data cannot be written.
Strm Start NG	Timeout of system packet input at the beginning	Rzn Rsv NG	R Zone Reserve failed.
IN Encode	Changes cannot be made in the process of encoding.	Rzn Cls NG	R Zone Close failed.
EncModul Hang	Encoder routine is hung up.	Rzn Rpr NG	R Zone Repair failed.
Ourob Strm NG	Inappropriate stream data to the Ouroboros input	Bdr Opn	Open Border failed.
BUF Overflow	Overflow of stream buffer	Bdr Cls	Close Border failed.
Drive Hang	Drive is hung up.	Format NG	Formatting failed.
Write Err	The drive failed to write and could not be recovered.	OPC NG	OPC failed.
Read Err	Reading failed, ECC failed, etc.	PCA Full	PCA has been used up.
Drv Hard Err	Abnormality in the drive hardware or firmware	RMA Full	RMA has been used up.
Mech No Res	No response from the mechanical U-Com	SW Vrec mode	Switching to video recording routine is required.
Drv TimeOut	Timeout for drive operation	SW Vpb mode	Switching to video playback routine is required.
NWA Exhaust	NWA surpassed and impossible to be used	Something	Something is wrong.
MKB Invalid	MKB reading error	Status NG	Abnormality in change of statuses
Drv Err	General error of the drive	Irr Action	Incorrect action
DISC Full	No further data can be written because the disc is full.	Abort	Cancellation
No More Info	No more space in the internal work management area	I am Down	A request to turn off the power was placed.
No Perm	No permission to write to the disc	Repair Exec	Repairing has been executed.
Limit Over	Standard maximum limit was over.	Format Exec	Formatting has been executed.
Rec Pause	No operation permitted during recording pause	BUG	Some bugs

Table 7.2 Description of VR recording-related errors

Note:

[REFERENCE]

ECC=4 Byte code for error correction ,
NWA=Next Writable Address ,
MKB= Media Key Block ,

UDF=Universal Disc Format , VMG=Video Manager , TMP_VMGI=Temp Video Manager Information,

PCA= Power Calibration Area , RMA=Recording Management Area , Border=from Lead-in to Lead-out ,

OPC=Optical Power Control

^{*} A dark halftone dot meshing part is an error of the MPEG Encoder, and a light halftone dot meshing part is an error of the drive system.

^{*} When the drive system is errored, there is a problem in crack and dirt of the disc or drive oneself (pickup is dirty).

7.1.4 SERVICE MODE

1. Error Rate Measurement

• How to Enter this Mode: Press the [ESC] and [SIDE-B] buttons sequentially.

Functions: When enter this mode, measure the error rate automatically.

1 VR mode record

Record it for 10 seconds and playback the title.

During the playback and stop, display the error rate in FL and OSD.

ERR RATE : *.**E-*

Video mode record

Record it for 30 seconds and playback the title.

During the playback and stop, display the error rate in FL and OSD.

ER (av):*.*E-* * (Display - during measurements)

③ DVD-VIDEO playback

Playback, and measure the error rate and display it. Stop afterwards.

ER (av):*.*e-* * (Display - during measurements)

4) CE

Trace it from the lead of track 1 and display the error rate.

E. RATE:*.*e-*

• How to Release: Press the [ESC] button to release from this mode.

2. Error Rate Measurement During DVD-VIDEO Playback

• How to Enter this Mode: Press the [ESC] and [n] buttons sequentially during playback. (n: Numeric button)

Functions: When enter this mode, measure the error rate of DVD-VIDEO and display it.

Record it for 10 seconds and playback the title.

ER (av):*.*e-* * (Display - during measurements)

• How to Release: Press the **[ESC]** button to release from this mode.

3. VR Aging Mode

How to Enter this Mode: Press the [ESC] and [REP.B] buttons sequentially to enter the aging mode.
 Display [AGING] on the left part of FL and display loop count on the right part of FL during this mode.

Functions: When enter this mode, repeat the following operations automatically.

- ① VR initialization
- 2 Video recording 60 minutes
- 3 Playback 45 minutes
- 4 Tray open
- 5 Tray close

Display the following counts in FL during the aging mode.

[AGING 0001]

• How to Release : Press the **[ESC]** button to release from this mode.

Note: Aging Mode stops when an error occurs. Press the **[ESC]** button to release from this mode. And see the error history with Debugging Mode.

4. Version Display

- How to Enter this Mode: Press the [ESC] and [FRM/TIM] buttons sequentially to display the version information screen.
- How to Release: Press the [ESC] button to release from this mode. (screen disappears)

5. Version Display (for Remote Control Unit of Accessory)

How to Enter this Mode: Perform highlight display the position of "main unit setting / voice output / digital output / ON", and press the [ANGLE] button of the remote control unit of accessory.

The following display appears at a position of the third layer.

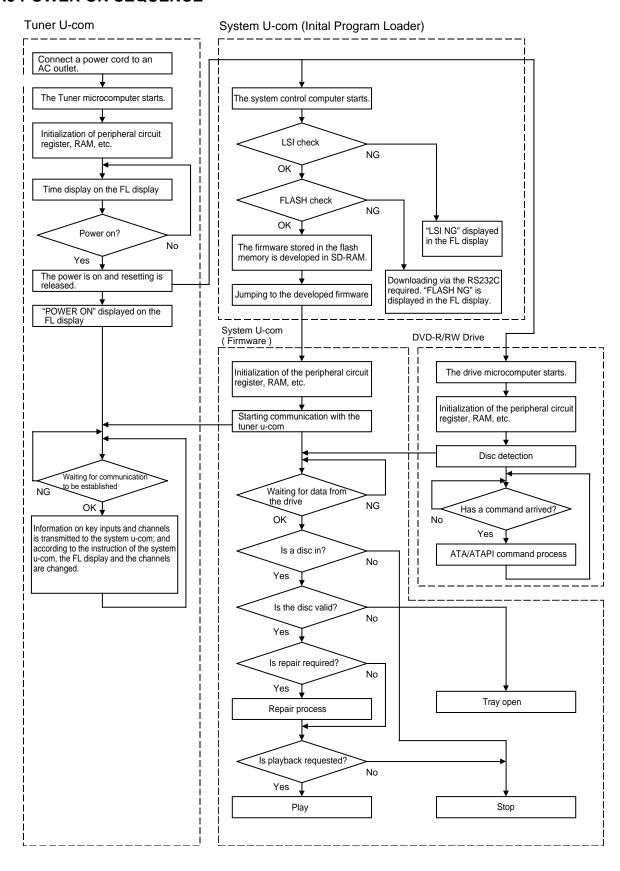
SYSCON: RELEASE_112
TUFLCON: 1.5200 *
DRIVE: 1.61C *
DEVICE: AV1=ES6.0

6. FL All Lighting Mode

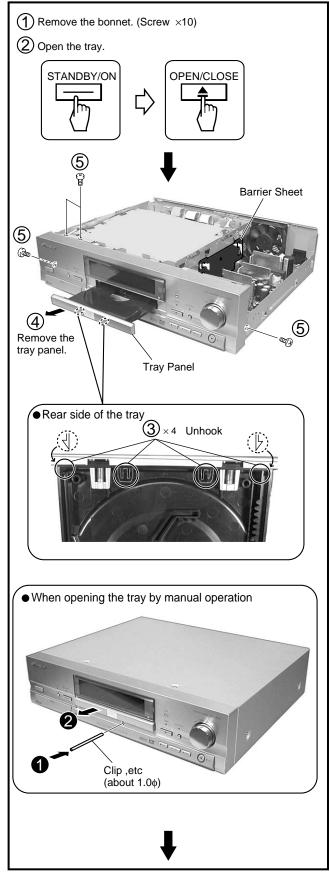
- How to Enter this Mode: All FL lights when pressing the [ESC] and [TEST] buttons sequentially.
- How to Release : Press the **[ESC]** button to release from this mode. (Return to normal display.)

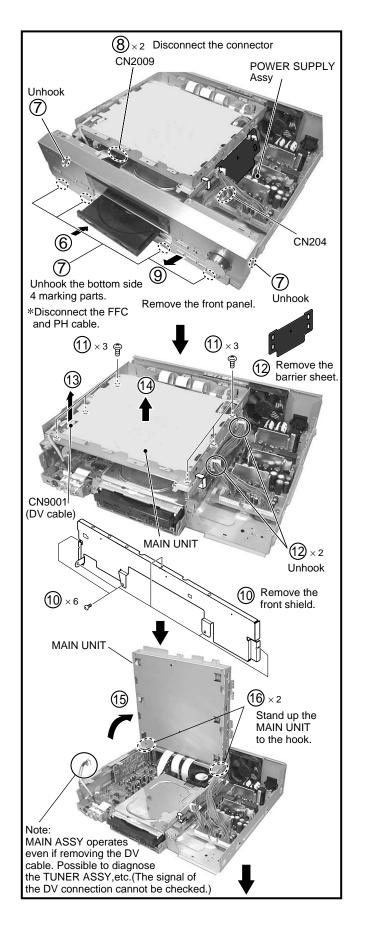
Note: Take care not to light all FL Tube for long time.

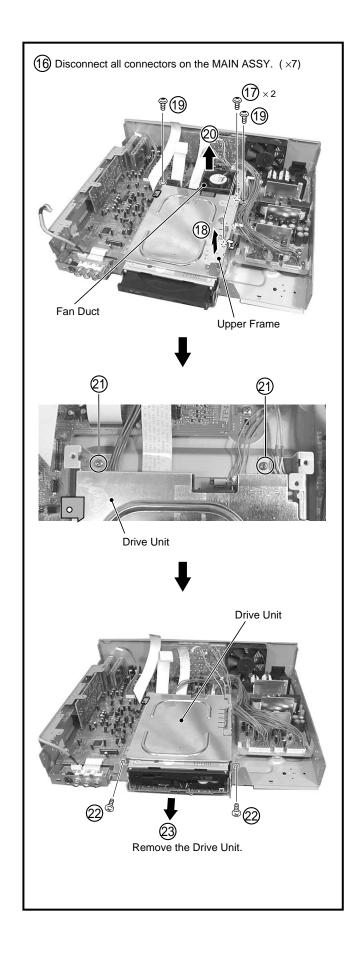
7.1.5 POWER ON SEQUENCE



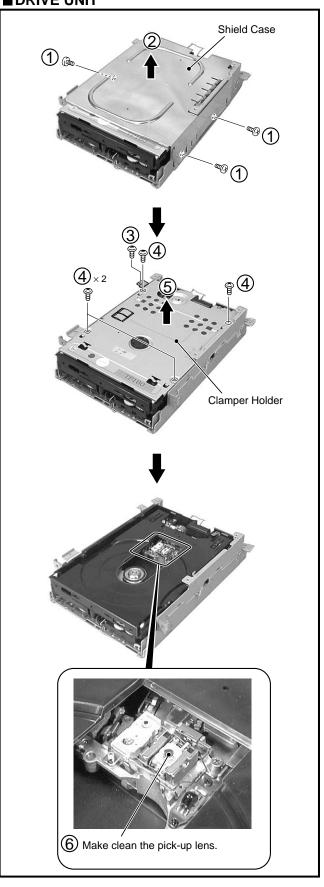
7.1.6 DISASSEMBLY



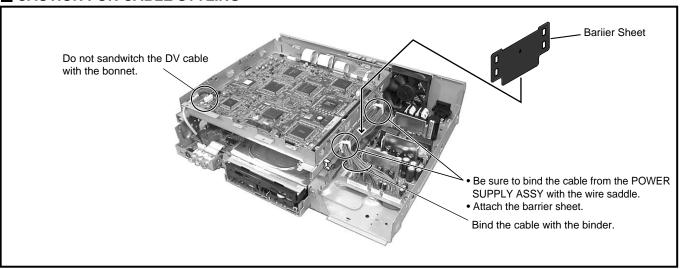




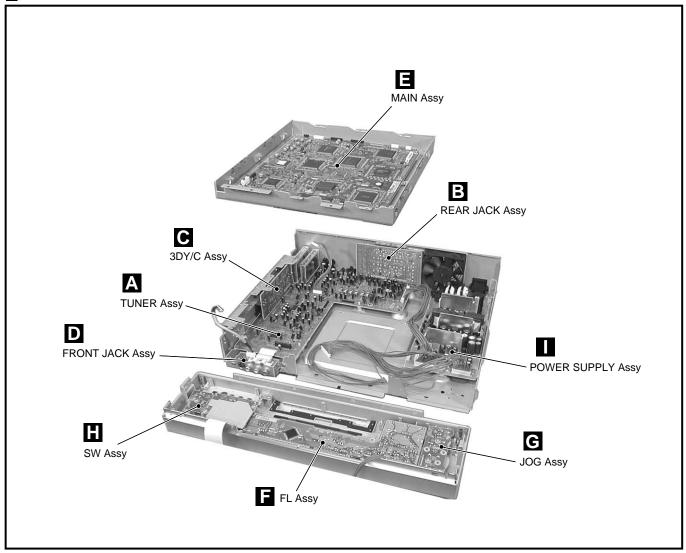
■ DRIVE UNIT



■ CAUTION FOR CABLE STYLING



■ PCB BOARD LOCATION



7.2 IC

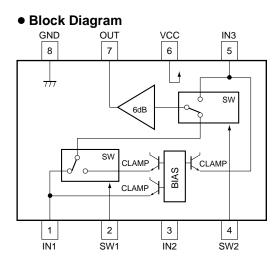
• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

List of IC

MM1118XF, TK15452V, TK15453V, BA7665FS, PE5275, RV5C386A, CXA2094Q, LC7454M, HD6417709AF100B, PE5219A, PD6342A, DVXCEL-BA1, UPD61003, PE7004A, CS8420-CS, TC9412AF, PD0272A, TSB42AB4PDT, TSB41AB2PAP, PE7003B, PDY078A, UPD65954-GC-E59-7EA

■ MM1118XF (TUJB ASSY: IC1003, IC1004, IC1171)

Video Switch IC



• Truth Table

SW1	SW2	OUT			
L	L	IN1			
Н	L	IN2			
_	Н	IN3			

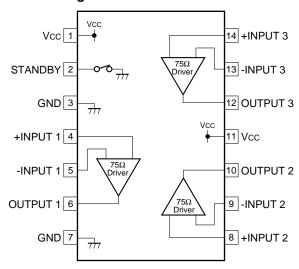
Pin Function

No.	Pin Name	Function
1	IN1	Input (1)
2	SW1	Switch (1)
3	IN2	Input (2)
4	SW2	Switch (2)
5	IN3	Input (3)
6	Vcc	Power supply
7	OUT	Output
8	GND	Ground

■ TK15452V (TUJB ASSY : IC1311)

Video Amplifier IC

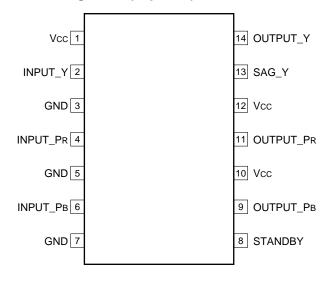
Block Diagram



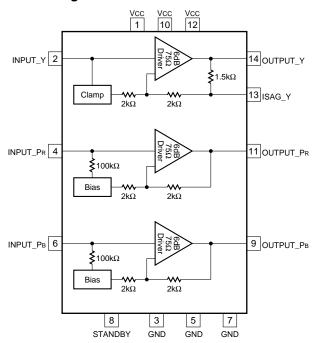
■ TK15453V (TUJB ASSY : IC1312)

• Video Amplifier IC

• Pin Assignment (Top view)



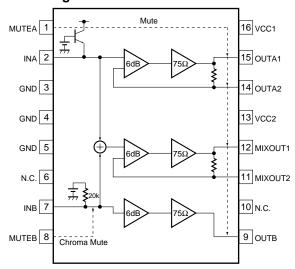
Block Diagram



■ BA7665FS (TUJB ASSY : IC1351)

• Video IC

Block Diagram



Pin Function

No.	Pin Name	1/0	Pin Function
1	MUTEA	ı	Mute control pin
2	INA	ı	Composite Y signal input pin
3	GND	_	Ground
4	GND	-	Ground
5	GND	-	Ground
6	N.C.	_	Non connection
7	INB	ı	Chroma signal input pin
8	MUTEB	- 1	Mute control pin
9	OUTB	0	Chroma signal output pin
10	N.C.	-	Non connection
11	MIXOUT2	0	Y/C MIX signal output pin
12	MIXOUT1	0	Y/C MIX signal output pin
13	VCC2	_	Power supply pin
14	OUTA2	0	Composite Y signal output pin
15	OUTA1	0	Composite Y signal output pin
16	VCC1	-	Power supply pin

■ PE5275 (TUJB ASSY : IC2003)

• Tuner Control Microcomputer

• Pin Function (1/2)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
1	P120	TIMER	0	LED for timer	41	P21	TXD1	0	MAIN communication line
2	P121	DVDLED	0	DVDLED	42	P22	ASCK1	I	
3	P122	FLOFF	0	For FL OFF	43	P23	TUREQ	0	Communication request of tuner control IC
4	P123	DOLBY	0	LED for FL DOLBY	44	P24	WRTPRT	0	EEPROM writing permission
5	P124	FLCS	0	FL Driver communication line	45	P25	SDAM	I/O	I2C data input/output
6	P125	XFLRST	0	FL DRIVE reset signal	46	P26	XRESET	0	RESET OUT
7	P126	JOGA	ı	FL JOG input	47	P27	SCLM	0	I2C clock input
8	P127	JOGB	ı	FL JOG input	48	P80	IOC	0	Data input/output control signal of LC7454
9	VDD	VDD	_	Power supply	49	P81	SLICE	I	Pulse output at XDS specification line
10	X2	X2		Connect a 6MHz ceralock	50	P82	NC	_	NC
11	X1	X1	Ľ	Cormect a Givin iz certaioux	51	P83	P_ON	0	POWER ON signal
12	Vss	Vss	-	Ground	52	P84	NC	_	NC
13	XT2	XT2	ļ ,	32k input	53	P85	NC] _	
14	XT1	XT1] '	152K IIIput	54	P86	NC	-	NC
15	XRESET	XRESETIN	I	Reset IC input	55	P87	TUSEL1	0	Salact the ground ways or PS
16	P00	TUACK	1	MAIN communication line	56	P40	TUSEL2		Select the ground wave or BS
17	P01	XINTRA	١.	DTO a service di se	57	P41	GOSTCS	0	Gauguin peripheral chip select
18	P02	XINTB	I	RTC communication	58	P42	XCVBS	0	S composite select
19	P03	NC	-	NC	59	P43	XTUMTE	0	Video mute at input switch to George
20	P04	NSTD	I	3-dimensional non-standard detection	60	P44	X3D	0	3-dimensional Y/C select
21	P05	LN26	ı	Both fields are 32 μpulses with 26 LINE	61	P45	LINSEL1	0	External input switch 1
22	P06	NC	-	NC	62	P46	LINSEL2	0	External input switch 2
23	AVdd	AVdd	-	Power supply	63	P47	F_ON	0	ON/OFF signal for fan
24	AVRef0	A/D Ref	1	A/D reference voltage input	64	P50	BUSY	I	Braster BUSY signal
25	P10	KEY1		FL KEY input 1	65	P51	XDSCE	0	XDS chip enable
26	P11	KEY2] '	FL KEY input 2	66	P52	XDSCK	0	XDS clock
27	P12	SONYKEY1		Front panel key for SONY	67	P53	FANDET	I	FAN rotation detection
28	P13	SONYKEY2] '	Tion paner key for SONT	68	P54	TUON	0	Tuner ON
29	P14	NC	_	NC	69	P55	N3D	0	Forced 2D mode signal for three dimensions
30	P15	AFT	I	Ground wave tuning gap input	70	P56	SQEEZE	0	SQEEZE signal for D terminal and skirt
31	P16	THERMO	ı	Temperature detection input	71	P57	LET_S	0	LETTER signal for S terminal
32	P17	NC	_	NC	72	Vss	Vss	_	Ground
33	Avss	Avss	_	Analog ground	73	P60	OECFO	I	Field distinction pulse output H: Odd numbers
34	P130	VI_ON	0	Video circuit ON for LINE input	74	P61	CPDT	I	XDS data output
35	P131	RSTCTL	0	Reset mute signal for sag measures	75	P62	BLCS	0	Chip select signal for braster
36	AVRef1	D/A Ref	I	D/A reference voltage input	76	P63	REGION1	1	Region 1
37	P70				77	P64	REGION2	∟'	Region 2
38	P71	FLDATA		FL DRIVER communication line	78	P65	AV1RST	0	AV1 reset signal
39	P72	FLCP	0	LE DRIVER COMMUNICATION line	79	P66	XBLRST	0	Braster reset signal
40	P20	RXD1	I	MAIN communication line	80	P67	XSELCS	I	For S input detection/for S signal switch (EU)

DVR-7000

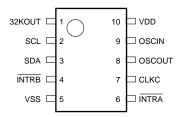
• Pin Function (2/2)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
81	VDD	VDD	_	Power supply	91	P35	SELIR	I	Remote control input
82	P100				92	P36			
83	P101				93	P37	XCHEKR	ı	Checker mode
84	P102				94	TEST	VPP	ı	VPP input for FLASH
85	P103				95	P90	MAKER1	ı	Manufacture identification code 1
86	P30				96	P91	FLDIM1	0	For FLDIMER
87	P31				97	P92	FLDIM2		FOI FEDIMER
88	P32				98	P93	REGION3	ı	Destination code 3
89	P33				99	P94	MAKER2	ı	Manufacture identification code 2
90	P34	CSSYNC	I	CSSYNC input for CSREC	100	P95	XSRVICE	I	Service mode

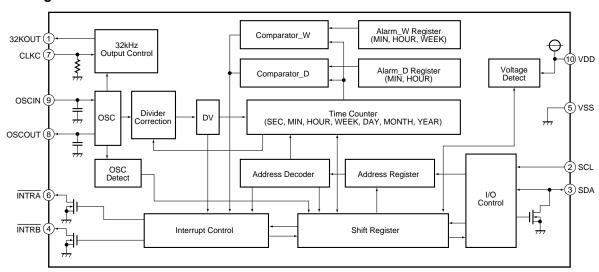
■ RV5C386A (TUJB ASSY : IC2008)

• Real Time Clock IC

• Pin Assignment (Top view)



Block Diagram

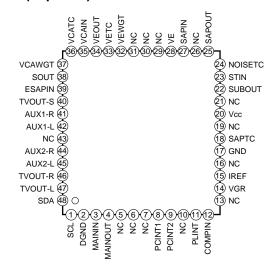


Pin Function

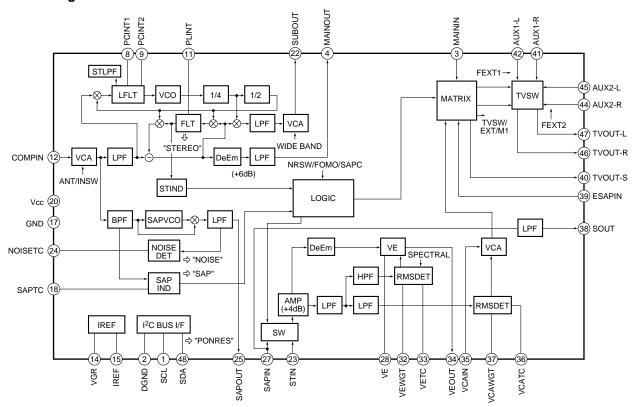
No.	Pin Name	I/O	Pin Function
1	32KOUT	0	32.768kHz clock output When rises up the power supply from 0V, output a clock if CLKC terminal is "H". In the CMOS output, CLKC terminal does not output it at the time of "L" or open.
2	SCL	I	Serial clock input Synchronize with this clock, and input and output data from the SDA terminal. As for this input, input is possible to 5.5V without relation in power supply voltage.
3	SDA	I/O	Serial input and output Synchronize in SCL, and input and output the writing data or readout data. As for this input, input is possible to 5.5V without relation in power supply voltage. The output is open drain.
4	ĪNTRB	0	Interrupt output B Output alarm interrupt (Alarm_W) for CPU. When rises up the power supply from 0V, it becomes off state. Nch open drain output.
5	VSS	-	Negative power supply input
6	INTRA	0	Interrupt output A Output alarm interrupt (Alarm_D) for CPU. When rises up the power supply from 0V, it becomes off state. Nch open drain output.
7	CLKC	I	Clock control input Control the 32KOUT output. At the time of "L" or open,32KOUT output fixed to "L". Pull-down resistor is built in. As for this input, input is possible to 5.5V without relation in power supply voltage.
8	OSCOUT	0	Oscillation circuit output Connect a 32.768kHz crystal resonator.
9	OSCIN	I	Oscillation circuit input Connect a 32.768kHz crystal resonator.
10	VDD	_	Positive power supply input

■ CXA2094Q (TUMJ ASSY : IC4601)

- Multi-channel Decoder IC
- Pin Assignment (Top view)



Block Diagram

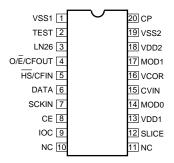


• Pin Function

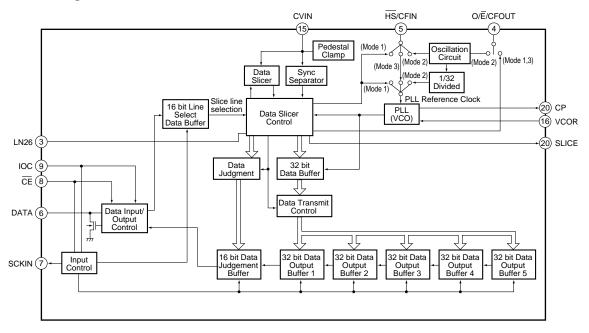
No.	Pin Name	I/O	Pin Function
1	SCL	I	Serial clock input
2	DGND	_	Digital ground
3	MAININ	I	Inputs L+R signal from MAINOUT of pin 4
4	MAINOUT	0	L+R signal output
5	NC	-	NC
6	NC	_	NC
7	NC	_	NC
8	PCINT1	_	Internal via of DI I loop filter on the stores block
9	PCINT2	_	Integral pin of PLL loop filter on the stereo block
10	NC	-	NC
11	PLINT	_	Integral pin of loop filter on the pilot cancel circuit
12	COMPIN	I	Multiplex signal input
13	NC	-	NC
14	VGR	0	Band gap reference output
15	IREF	-	Reference current setting pin for filter and VCO
16	NC	_	NC
17	GND	_	Analog ground
18	SAPTC	_	Time constant setting pin for SAP carrier detection circuit
19	NC	_	NC
20	Vcc	_	power supply
21	NC	_	NC
22	SUBOUT	0	L-R signal output
23	STIN	I	Inputs L-R signal from SUBOUT of pin 22
24	NOISETC	_	Time constant setting pin for NOISE detection circuit
25	SAPOUT	0	FM detector output of SAP
26	NC	_	NC
27	SAPIN	ı	Inputs SAP signal from SAPOUT of pin 25
28	VE	-	Integral pin of valiable deemphasis
29	NC	-	NC
30	NC	-	NC
31	NC	_	NC .
32	VEWGT	_	Weight pin of effective-value detector circuit of variable deemphasis control
33	VETC	_	Pin to decide the return time-constant of effective-value detector circuit of variable deemphasis control
34	VEOUT	0	Variable deemphasis output
35	VCAIN	ı	VCA input
36	VCATC	_	Pin to decide the return time-constant of effective-value detector circuit of VCA control
	VCAWGT	_	Weight pin of effective-value detector circuit of VCA control
38	SOUT	0	Simple SAP output
	ESAPIN	I	Inputs a signal from SOUT of pin 38
40	TVOUT-S	0	Rear output Outputs monaural or simple SAP
41	AUX1-R	I	R ch external input (1)
42	AUX1-L	ı	L ch external input (1)
43	NC	_	NC
44	AUX2-R	I	R ch external input (2)
45	AUX2-L	I	L ch external input (2)
46	TVOUT-R	0	R ch output of TVOUT
47	TVOUT-L	0	L ch output of TVOUT
48	SDA	I/O	Serial data input/output

■ LC7454M (TUMJ ASSY : IC5001)

- CMOS Data Slicer
- Pin Assignment (Top view)



Block Diagram



Operation on Each Mode

The LC7454M has three operating modes. The operation mode can be selected by the status of MOD0 and MOD1 terminals. The functionality of three modes is the same. Only the PLL reference frequency which is used to generate the internal operation clock is different. Use model or mode3 only in the application which is used to generate the internal operation clock is different. Use model or mode3 only in the application which uses 2x data. Any mode (Mode1, 2 and 3) can be used in the 1x data only application.

Pin	Pin Name		Applications	PLL Reference
MOD1	MOD0	WIOGE	Applications	I LL Neielelice
Open	Open	Mode 1	NTSC-VCR	Use H-sync signal which is separated from C-Video signal.
Open	VDD	Mode 2	NTSC-VCR	Use 1/32 divided signal 503kHz which is generated by external ceramic resonator.
VDD	Open	Mode 3	NTSC-TV	Use H-sync signal from Fly Back.

• Pin Function

N.	Din Nama		Pin Function							
No.	Pin Name	Mode 1	Mode 2	Mode 3						
1	VSS1	Ground	Ground							
2	TEST	Test pin, open in normal operation.								
3	LN26	32 μs pulse output at line 26 timing	on both field.							
4	O/XE/CFOUT	Pulse output for field judgment *1	Output pin for ceramic resonator	Pulse output for field judgment *1						
5	XHS/CFIN	Sync separated XHS pulse output	Input pin for ceramic resonator	External XHS pulse input						
6	DATA	Line select data input and slice data	a output *2							
7	SCKIN	Data transmit clock input								
8	XCE	Chip select input *3								
9	IOC	Data direction control signal input *	Data direction control signal input *4							
10	NC	NC								
11	NC	NC								
12	SLICE	Pulse output at selected slice line								
13	VDD1	Power supply								
14	MOD0	Open	Connect to VDD	Open						
15	CVIN	Composite video input								
16	VCOR	Connect resistor for internal VCO o	scillation frequency control							
17	MOD1	Open	Open	Connect to VDD						
18	VDD2	Power supply								
19	VSS2	Ground								
20	СР	Filter pin for internal PLL								

^{*1: &}quot;H" level in Odd field, "L" level in Even field.

^{*2:} N-ch open drain in output mode.
*3: For chip select input, apply the "L" level only when data transmission is in effect.

If CE="H", data terminal will be input/output disabled, and SCKIN terminal will be input disabled.
*4: "H" level: Output mode, "L" level: Input mode

■ HD6417709AF100B (MAIN ASSY : IC1010)

• MPU IC

• Pin Function (1/3)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
1	MD1	SHMD1	- 1	CLK mode setting	41	D9	D9		
2	MD2	SHMD2	'	CER mode setting	42	D8	D8	I/O	Data bus
3	1.9V				43	D7	D7	"	Data bus
4	XTAL2	XTAL2	0	For RTC	44	D6	D6		
5	EXTAL2	EXTAL2	ı	FOIRIC	45	GND		_	Ground
6	GND (RTC)		_	Ground	46	D5	D5	I/O	Data bus
7	NMI	NMI	- 1	NMI interruption (Pull up)	47	VCCQ			
8	IRQ0	XIRQ0		AV1 interruption (Pull up)	48	D4	D4		
9	IRQ1	XIRQ1		Av i interruption (Full up)	49	D3	D3		
10	IRQ2	XIRQ2	1	Dvxcel interruption (Pull up)	50	D2	D2	1/0	Data bus
11	IRQ3	XIRQ3		Audery interruption (Pull up)	51	D1	D1		
12	IRQ4	XIRQ4		AV-1 (2nd) interruption	52	D0	D0		
13	D31	D31			53	A0	A0		
14	D30	D30			54	A1	A1		Address bus
15	D29	D29],,	Doto huo	55	A2	A2	0	Address bus
16	D28	D28	I/O	Data bus	56	A3	A3		
17	D27	D27			57	GND		_	Ground
18	D26	D26			58	A4	A4	0	Address bus
19	GND		-	Ground	59	VCCQ			
20	D25	D25	I/O	Data bus	60	A5	A5		
21	VCCQ				61	A6	A6		
22	D24	D24			62	A7	A7		Address bus
23	D23	D23			63	A8	A8		
24	D22	D22	I/O	Data bus	64	A9	A9	0	
25	D21	D21			65	A10	A10		
26	D20	D20	1		66	A11	A11		
27	GND		-	Ground	67	A12	A12		
28	D19	D19	I/O	Data bus	68	A13	A13		
29	1.9V				69	GND		_	Ground
30	D18	D18			70	A14	A14	0	Address bus
31	D17	D17	I/O	Data bus	71	VCCQ			
32	D16	D16			72	A15	A15		
33	GND		_	Ground	73	A16	A16		
34	D15	D15	I/O	Data bus	74	A17	A17		
35	VCCQ				75	A18	A18	0	Address bus
36	D14	D14			76	A19	A19		
37	D13	D13			77	A20	A20		
38	D12	D12	I/O		78	A21	A21		
39	D11	D11			79	GND		-	Ground
40	D10	D10			80	A22	A22	0	Address bus

• Pin Function (2/3)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
81	1.9V				121	BACK		0	Not used (TP)
82	A23	A23	0	Address bus	122	BREQ		I	Not used (Pullup, TP)
83	GND		-	Ground	123	WAIT	XWAIT	I	Wait input (Pullup)
84	A24	A24	0	Address bus	124	RESETM	XRESET	I	Manual reset input (Pullup)
85	VCCQ				125	PTH5			(TP)
86	A25	A25	0	Address bus	126	PTG7			(TP)
87	BS	XBS	0	Bus cycle start signal	127	ASEMD0	ASEMD0	I	For H-UDI
88	RD	XRD	0	Read strobe	128	ASEBRKAK	ASEBRKAK	0	(AUD correspondence)
89	WE0	XWE0			129	PTG4			(TP)
90	WE1	XWE1			130	AUDATA3	AUDATA3	_	For H-UDI
91	WE2	XWE2	0	Write strobe	131	AUDATA2	AUDATA2	0	(AUD correspondence)
92	WE3	XWE3]		132	GND		_	Ground
93	RD/WR	RDWR	0	Read / Write	133	AUDATA1	AUDATA1	0	For H-UDI (AUD correspondence)
94	AUDSYNC	AUDSYNC	0	For H-UDI (AUD correspondence)	134	1.9V			
95	GNDQ				1	AUDATA0	AUDATA0	0	For H-UDI (AUD correspondence)
96	CS0	XCS0	0	Chip select 0	-	TRST	TRST		FartHUDI
97	VCCQ				137	TMS	TMS		For H-UDI (AUD correspondence) (pullup)
98	CS2	XCS2		Chip select 2	138		TDI	•	
99	CS3	XCS3		Chip select 3	139	TCK	TCK		
100	CS4	XCS4	0	Chip select 4	140	PINT11	PINT11		Slalom interruption (Pullup)
	CS5	XCS5		Chip select 5		PINT10	PINT10	ı	(Pullup, TP)
	CS6	XCS6		Chip select 6	-	PINT9	PINT9		WM interruption (Pullup)
103	PTE4	DVOEN	0	DV Req Mask	143	PINT8	PINT8		Slalom interruption (Pullup)
	PTE5	SELVCD	0	Audio CLK switching control signal for V-CD	144	MD0	SHMD0	I	CLK mode setting
	CKE	CKE	0	CKE for SDRAM	-	1.9V			
	RAS3L	XRAS3L	0	RAS for SDRAM	146	CAP1	CAP1	_	For PLL
	PTJ1		I/O		147	GND (PLL1)		_	Ground
108	CAS	XCASLL	0	CAS fro SDRAM	148				
109	GNDQ				_		CAP2	_	For PLL
110	PTJ3	XRSTPH	0	Reset output for 1394phy	150	1.9V			
	vccq				-	AUDCK		0	For H-UDI (AUD correspondence)
	PTJ4		1/0	I/O port for debugging (TP)		GND		_	Ground
	PTJ5			per let dezagging (11)	_	GND			0.000
	DACK0	XDACK0	0	DMA ACK for Slalom/BY-chip	_	1.9V			
	DACK1	XDACK1	0	DMA ACK for Vaikilt	_	XTAL	XTAL	0	CPU clock
116	PTE6	XRSTVQ	0	Reset output for VQE	156	EXTAL	EXTAL	ı	CPU clock
	PTE3	XDARST	0	Reset output for audio DAC		PTJ6	TUACK	0	Communication ACK signal of Tuner Control Microcomputer
	PTE2	XRSTAU	0	Reset output for Audery	_	PTJ7	EDSEL	0	Bus switching signal for WM
119	PTE1	XRSTX	0	Reset output for DVxcel	159	TCLK		I/O	Clock I/O for TMU/RTC (TP)
120	TDO	TDO	0	For H-UDI (AUD correspondence)	160	IRQOUT		0	Not used (TP)

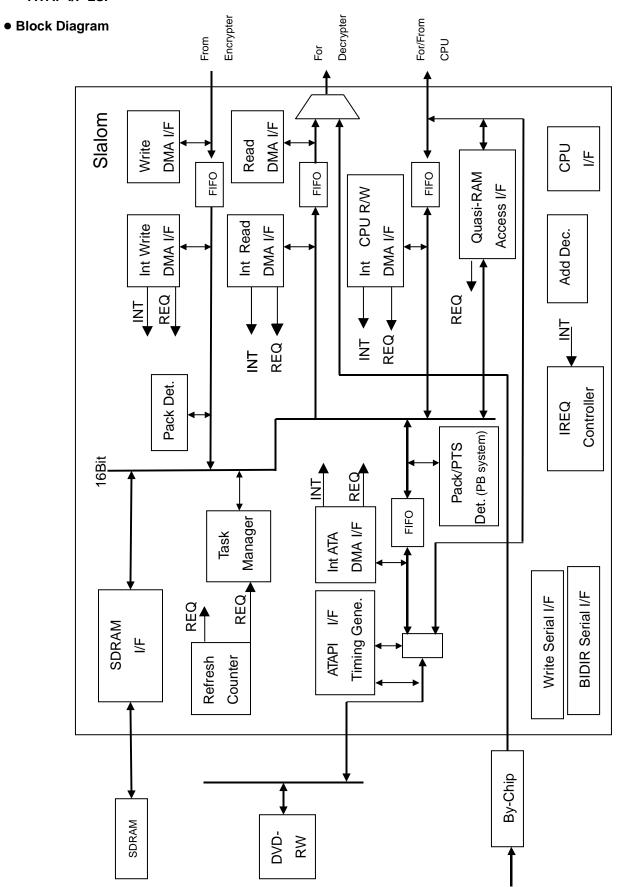
DVR-7000

• Pin Function (3/3)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
161	GND		_	Ground	185	PINT3	PINT3	ı	1394celinx interruption
162	CKIO	CKIO	I/O	System clock I/O	186	PINT2	PINT2	ı	Ouroboros interruption
163	VCCQ				187	PINT1	TUREQ	ı	Tuner Control Microcomputer communication interruption
164	TXD0	TXD0	0	For Tuner Control Microcomputer	188	PINT0	PINT0	ı	George VSYNC INT (Pull up)
165	SCK0	SCK0	0	For runer Control Microcomputer	189	PTD1		0	LED output for debugging
166	TXD1	TXD1	0	For RS232C	190	PTD0			LED dulput for debugging
167	SCK1	SCK1	0	(TP)	191	DREQ0	DREQ0	I	DMA REQ for Slalom/By-chip
168	TXD2	TXD2	0	(For professional video)	192	DREQ1	DREQ1	I	DMA REQ for Vaikit
169	SCK2	SCK2	0	(TP)	193	RESETP	XRESETP	ı	Power on reset input
170	RTS2	RTS2	0	(For professional video)	194	CA	CA	I	Chip active
171	RXD0	RXD0	0	For Tuner Control Microcomputer	195	MD3	SHMD3		Bus width setting for area 0
172	RXD1	RXD1	0	For RS232C	196	MD4	SHMD4	'	Bus width setting for area o
173	GND		_	Ground	197	MD5	SHMD5	I	Endian setting
174	RXD2	RXD2	1	(For professional video)	198	AGND		_	Analog ground
175	1.9V				199	PTL0	DBP0	ı	Audery DBP0
176	CTS2	XIRQ5	- 1	(For professional video)	200	PTL1	DBP1	1	Audery DBP1
177	PINT7	PINT7		By-chip interruption (Pull up)	201	PTL2	DBP2	1	Audery DBP2
178	PINT6	PINT6	'	By-criip interruption (Full up)	202	PTL3	DBP3	1	Audery DBP3
179	PINT5	PINT5		Vaikilt interruption (Pull up)	203	PTL4	SRCPT	1	SRC lock signal
180	PINT4	PINT4	'	Valkiit interruption (Full up)	204	PTL5		1	(TP)
181	GND		_	Ground	205	AVCC			
182	PTD3		0	LED output for debugging	206	PTL6	VKGUI_T	ı	(TP)
183	VCCQ				207	PTL7	DVLOCK	ı	PLL lock judge signal for DV
184	PTD2		0	LED output for debugging	208	AGND		_	Analog ground

■ PE5219A (MAIN ASSY: IC3003)

• ATAP I/F LSI



• Pin Arrangement

٨	AVDATA 2	CLK27M	GND	DVDREQ	IDT	DVDATA 5	DVDATA 3	DVDATA 0	CS21B	VDD	CS4A0	GND	NEWWE1	NEWRD	EXT WAIT2	EXT WAIT0	GND	TEST8	TEST4	TEST0
M	AVDATA 5	TRST	GND	AVDATA 0	DVDACK	DVDATA 6	VDD	DVDATA 1	CS21A	CS2A2	CS4A1	CS5A2	NEWWEO NEWWE1	EXT WAIT3	EXT WAIT1	VDD	TEST7	TEST3	TEST2	VRCLK
>	AVDACK	AVDATA 4	AVDATA 3	AVDATA 1	TMS	DQT	DVDATA 4	DVDATA 2	CS2A0	CS2A3	CS4A2	CS5A5	VDD	GND	SHDIR	MCLK 27M	TEST6	TEST1	VRDATA	SR DATAI
n	AVDREQ	ΣĘ	AVDATA 7	GND	CLK27 MO	VDD	DVDATA 7	GND	GND	VDD	CS4A3	CS5A6	GND	SHBENB	VDD	TEST5	GND	VRCS	GND	SRCS
T	SHDREQ	SHIRQS	SHWAIT	AVDATA 6													SR DATAO	SRCLK	ATARST	GND
æ	SHCS2	GND	SHIRQ	VDD													VDD	ATA DATA14	ATA DATA13	ATA DATA12
٩	SHCS5	SHCS4	RST	SHDACK													ATA DATA15	ATA DATA11	ATA DATA10	GND
z	SHWE1	SHWE0	SHRDWR	GND													GND	ATA DATA9	ATA DATA8	ATA DATA7
W	SHADD 3	SHADD 2	SHADD 1	SHRD													ATA DATA6	ATA DATA5	ATA DATA4	ATA DATA3
٦	SHADD 7	SHADD 6	SHADD 5	SHADD 4													VDD	GND	ATA DATA2	ATA DATA1
Ж	SHADD 8	SHADD 10	SHADD 9	VDD													VDD	ATAADD 1	ATAADD 2	ATA DATA0
٦	SHADD 11	SHADD 12	SHADD 13	SHADD 14													ATAIRQ	ATACS0	ATAIORD ATACS1	ATAADD 0
н	SHADD 15	SHADD 16	SHADD 17	GND													GND	ATA	ATAIORD	GND
9	SHADD 18	SHADD 19	SHADD 20	SHADD 24													Z F	ATA IORDY	ATA DACK	ATA DREQ
ч	SHADD 21	SHADD 22		VDD													VDD	TEB	ATAOE	VDD
3	GND	SHADD 25	SHDATA 1	SHDATA 2													BYDATA 5	BYCPU ACK	BYCPU REQ	ATADIR
q	SHDATA 0	SHDATA 3	SHDATA 4	GND	SHDATA 9	VDD	SDADD 4	GND	SDADD 10	SDADD 13	VDD	DQML	GND	SDDATA 11	VDD	SDDATA 1	GND	BYDATA 6	BYDATA 7	BYDREQ
Э	GND	0)		ر د ا	ααΛ	SHDATA 15	SDADD 2	SDADD 7	SDADD 9	SDCS	SDCKE	DQMU	SDDATA 8	SDDATA 5	0,	ADD	SDDATA 15	BYDATA 1	BYDATA BYDATA 3	BYDACK
В	SHDATA 5	CLK40M SHDATA 8	SHDATA 7		SHDATA 14	SDADD 5	SDADD 1	SDADD 0	SDADD 12	GND	SDRAS	SDWR		SDDATA 9	SDDATA 4	SDDATA 12	SDDATA 0	SDDATA CLK54M BYDATA	BYDATA 2	BYDATA BYDATA 0 4
٧	GND	CLK40M		SHDATA 13	SDADD 3	SDADD 6	GND	SDADD 8	SDADD 11	CLK54 MO	GND	SDCAS	SDDATA 7		SDDATA 10	SDDATA 2	SDDATA 13	SDDATA 14	GND	BYDATA 0
	-	2	3	4	5	9	7	8	6	10	1	12	13	14	15	16	17	18	19	20

• Pin Function (1/2)

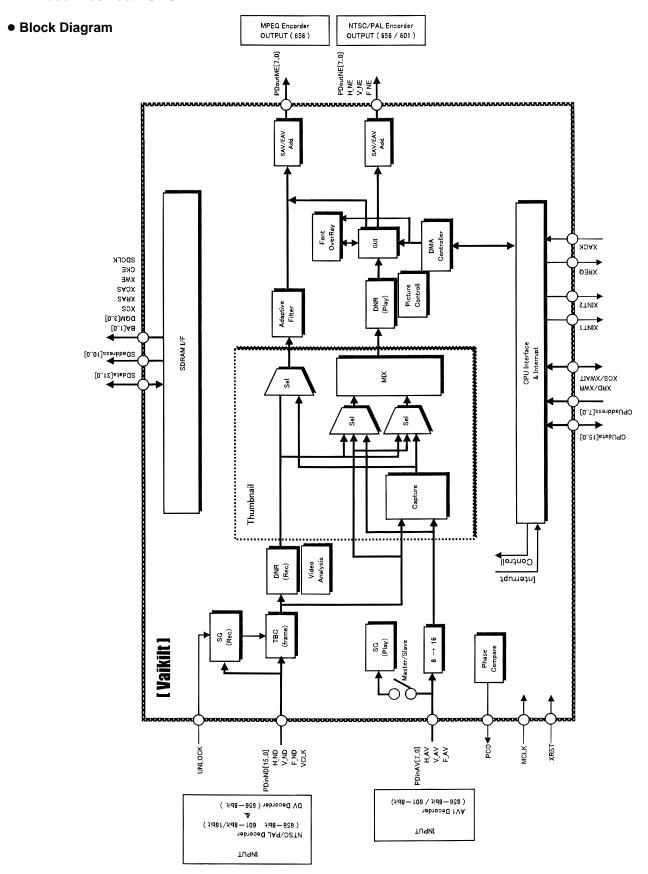
Pin Name	I/O	Function	Connection Point	Remarks
DQMU	0	Input mask / Output enable	SDRAM	
DVDATA	I	Data input	MPEG encoder	
DVDACK	0	DMA acknowledge	MPEG encoder	
DVDREQ	I	DMA request	MPEG encoder	
CLK27M	I	Clock input	Oscillation circuit	27MHz
CLK27MO	0	Clock output	MPEG encoder	27MHz
AVDATA	0	Data output	MPEG decoder	
AVDREQ	I	DMA request	MPEG decoder	
AVDACK	0	DMA acknowledge	MPEG decoder	
VRDATA	0	Data	Electric volume	
VRCLK	0	Clock output	Electric volume	
VRCS	0	Chip select/Data strobe	Electric volume	
SRDATAI	I	Data input	SRC	SRSSI
SRDATAO	0	Data outpit	SRC	SRSSO
SRCLK	0	Clock output	SRC	
SRCS	0	Chip select/Data strobe	SRC	SRXCS
EXTCS	0	Chip select	Peripheral device	CS2A0,
				CS21A,CS21B,
				CS2A3-2,CS4A3-0,
				CS5A2,CS5A6-5
NEWRD	0	Read	Peripheral device	
NEWWE	0	Write	Peripheral device	NEWWE1-0
EXTWAIT	I	Wait	Peripheral device	EXTWAIT3-0
SHBENB	0	Bus enable	Bus buffer	
SHDIR	0	Direction	Bus buffer	
MCLK27M	0	Clock output	George	27MHz
TEST	0	For TEST		TESTOUT8-0
TDI	I	JTAG		
TDO	0	JTAG		
TCK	I	JTAG		
TRST	1	JTAG		
TMS	I	JTAG		
TIN	I	For TEST	GND	
TEB	I	For TEST	VDD	

• Pin Function (2/2)

Pin Name	I/O	Function	Connection Point	Remarks		
SHDATA	I/O	Data	CPU			
SHADD	ı	Address	CPU			
SHRDWR	HRDWR I Read write		CPU			
SHRD	I	Read	CPU			
SHWE	I	Write	CPU	SHWE1-0		
SHCS	ı	Chip select	CPU	SHCS2,SHCS4,SHCS5		
SHDREQ	0	DMA request	CPU			
SHDACK	ı	DMA acknowledge	CPU			
SHIRQ	0	Interruption	CPU			
SHIRQS	0	Interruption	CPU			
SHWAIT	0	Wait	CPU			
RST	ı	System reset	CPU			
CLK40M	ı	Clock input	Oscillation circuit	40MHz (66MHz)		
ATARST	0	ATA reset	ATA device			
ATADATA	I/O	Data	ATA device			
ATAADD	0	Address	ATA device			
ATACS	0	Chip select	ATA device			
ATAIRQ	ı	Interruption	ATA device			
ATAIORD	0	Read	ATA device			
ATAIOWR	0	Write	ATA device			
ATADREQ	ı	DMA request	ATA device			
ATADACK	0	DMA acknowledge	ATA device			
ATAIORDY	ı	I/O ready	ATA device			
ATAOE	0	Output enable	Bus buffer	Not used		
ATADIR	0	Direction	Bus buffer	not used		
BYDATA	ı	Data input	BY-Chip			
BYDREQ	0	DMA request	BY-Chip	For Stream		
BYDACK	1	DMA acknowledge	BY-Chip	For Stream		
BYCPUACK	0	DMA acknowledge	BY-Chip	CPUDMA		
BYCPUREQ	ı	DMA request	BY-Chip	CPUDMA		
SDDATA	I/O	Data	SDRAM			
SDADD	0	Address	SDRAM	SDADD13-0		
SDCS	0	Chip select	SDRAM			
SDRAS	0	Row address strobe	SDRAM			
SDCAS	0	Column address strobe	SDRAM			
SDWR	0	Write	SDRAM			
CLK54M	ı	Clock input	Oscillation circuit	54MHz		
CLK54MO	0	Clock output	SDRAM	54MHz		
SDCKE	0	Clock enable	SDPAM			
DQML	0	Input mask / Output enable	SDRAM			

■ PD6342A (MAIN ASSY: IC4006)

• Video Pre / Post LSI IC



• Pin Function (1/7)

No.	Pin Name	I/O	Pin Function			
1	SDDATA22					
2	SDDATA21		CDDAM DATA IN/OUT			
3	SDDATA20	7 1/0	SDRAM DATA IN/OUT			
4	SDDATA19					
5	VSS	-	ND			
6	VDDI	-	Internal VDD: 2.5V			
7	SDDATA18					
8	SDDATA17	I/O	SDRAM DATA IN/OUT			
9	SDDATA16					
10	OVSSX0	_	Append GND			
11	OVDD3X0	-	Append interface VDD: 3.3V			
12	SDTEST7					
13	SDTEST6					
14	SDTEST5		SDRAM I/F TEST output			
15	SDTEST4	7	SDRAW I/F 1E31 Output			
16	SDTEST3					
17	SDTEST2					
18	VSS	-	GND			
19	VDDI	-	Internal VDD: 2.5V			
20	SDTEST1	0	SDRAM I/F TEST output			
21	SDTEST0	7	3510 WW 1/1 1201 Octput			
22	O-PDOUTNE7		VIDEO DATA output for NTSC (PAL) ENCODER CCIR656 (8bit, 27MHz) output			
23	O-PDOUTNE6	0				
24	O-PDOUTNE5					
25	VDDE	_	Interface VDD: 3.3V			
26	OVSSX1	-	Append GND			
27	O-PDOUTNE4					
28	O-PDOUTNE3		VIDEO DATA quitout for NTSC (DAL) ENCODED			
29	O-PDOUTNE2	0	VIDEO DATA output for NTSC (PAL) ENCODER CCIR656 (8bit, 27MHz) output			
30	O-PDOUTNE1		, , , , , , , , , , , , , , , , , , , ,			
31	O-PDOUTNE0					
32	VSS	_	GND			
33	OVDD3X1	0	Append interface VDD: 3.3V			
34	O-H-NE	0	HSYNC output for NTSC (PAL) ENCODER			
35	O-V-NE	0	VSYNC output for NTSC (PAL) ENCODER			
36	O-F-NE	0	FIELD output for NTSC (PAL) ENCODER			
37	I-LACT	I	Active line Flag input from VIDEO DECODER. 15Hz input from the DV.			
38	I-NONSTDIN	I	Non standard signal Flag input from VIDEO DECODER			
39	OVSSX2	_	Append GND			
40	VDDE	_	Interface VDD: 3.3V			

• Pin Function (2/7)

No.	Pin Name	I/O	Pin Function			
41	I-H-ND	ı				
42	I-V-ND	ı	Connect to GND			
43	I-F-ND	ı				
44	I-PDINND7		Input the decode output of NTSC or PAL VIDEO DECODER			
45	I-PDINND6	'	CCIR656 (8bit, 27MHz) input			
46	VSS	_	GND			
47	VDDI	_	Internal VDD: 2.5V			
48	VCLK	I	27MHz CLK input			
49	I-PDINND5					
50	I-PDINND4					
51	I-PDINND3	١.	Input the decode output of NTSC or PAL VIDEO DECODER			
52	I-PDINND2	ı	CCIR656 (8bit, 27MHz) input			
53	I-PDINND1					
54	I-PDINND0					
55	I-PDINDV7					
56	I-PDINDV6		Input the decode output of DV I/F DECODER			
57	I-PDINDV5		CCIR656 (8bit, 27MHz) input			
58	I-PDINDV4					
59	VSS	_	GND			
60	VDDI	_	Internal VDD: 2.5V			
61	I-PDINDV3					
62	I-PDINDV2	١.	Input the decode output of DV I/F DECODER			
63	I-PDINDV1	'	CCIR656 (8bit, 27MHz) input			
64	I-PDINDV0					
65	I-CPUADDRESS8					
66	I-CPUADDRESS7					
67	I-CPUADDRESS6	١.	ODU ADDREGO i vest e 40k%			
68	I-CPUADDRESS5	'	CPU ADDRESS input * 16bit			
69	I-CPUADDRESS4					
70	I-CPUADDRESS3					
71	XRST	I	Hardware reset input			
72	VSS	_	GND			
73	I-XACK	I	Acknowledge input at DMA tranmission			
74	VDDI	_	Internal VDD: 2.5V			
75	I-CPUADDRESS2					
76	I-CPUADDRESS1	ı	CPU ADDRESS input * 16bit			
77	I-CPUADDRESS0					
78	I-XWR	ı	Write input from the CPU			
79	VDDI	_	Internal VDD: 2.5V			
80	OVSSX3	-	Append GND			

DVR-7000

• Pin Function (3/7)

No.	Pin Name	I/O	Pin Function			
81	I-XCS	1	Chip select input from the CPU			
82	I-XRD	ı	Read input from the CPU			
83	CPUDATA15	I/O	CPU DATABUS input/output			
84	VSS	-	GND			
85	VDDE	-	Interface VDD: 3.3V			
86	CPUDATA14					
87	CPUDATA13	1,/0	CDU DATADUS inquit/output			
88	CPUDATA12	1/0	CPU DATABUS input/output			
89	CPUDATA11					
90	OVSSX4	-	Append GND			
91	OVDD3X2	_	Append interface VDD: 3.3V			
92	CPUDATA10					
93	CPUDATA9] ,,	CPU DATABUS input/output			
94	CPUDATA8	1/0	CFO DATABOS ilipul/odiput			
95	CPUDATA7	1				
96	VSS	-	GND			
97	VDDE	-	Interface VDD: 3.3V			
98	CPUDATA6					
99	CPUDATA5] ,,	CPU DATABUS input/output			
100	CPUDATA4	1/0				
101	CPUDATA3					
102	OVSSX5	-	Append GND			
103	OVDD3X3	-	Append interface VDD: 3.3V			
104	CPUDATA2					
105	CPUDATA1	1/0	CPU DATABUS input/output			
106	CPUDATA0					
107	O-XREQ	0	Request output at DMA transmission			
108	VSS	-	GND			
109	VDDE	-	Interface VDD: 3.3V			
110	O-XIXT1	0	Interrupt output 1 to the CPU			
111	O-XIXT2	7 0	Interrupt output 2 to the CPU			
112	O-F-ME	0	FIELD output for MPEG ENCODER			
113	O-V-ME	0	VSYNC output for MPEG ENCODER			
114	VDDI	-	Internal VDD: 2.5V			
115	OVSSX6	-	Append GND			
116	O-H-ME	0	HSYNC output for MPEG ENCODER			
117	O-PDOUTME7		VIDEO DATA output for MPEG ENCODER			
118	O-PDOUTME6	0	CCIR656 (8bit, 27MHz) output			
119	VSS	-	GND			
120	O-PDOUTME5	0	VIDEO DATA output for MPEG ENCODER CCIR656 (8bit, 27MHz) output			

• Pin Function (4/7)

No.	Pin Name	I/O	Pin Function			
121	VDDI	-	Internal VDD: 2.5V			
122	O-PDOUTME4					
123	O-PDOUTME3					
124	O-PDOUTME2	0	VIDEO DATA output for MPEG ENCODER CCIR656 (8bit, 27MHz) output			
125	O-PDOUTME1		Contobo (obit, 27 mi iz) output			
126	O-PDOUTME0					
127	OVSSX7	-	Append GND			
128	OVDD3X4	-	Append interface VDD: 3.3V			
129	PLL-L	0	DIL TECT subsub ODEN			
130	PLL-FB	0	PLL TEST output: OPEN			
131	PCO	0	Phase comparison output of TBC			
132	TESTOUT7	0	TEST output of video system			
133	VSS	-	GND			
134	VDDI	-	Internal VDD: 2.5V			
135	TESTOUT6					
136	TESTOUT5					
137	TESTOUT4	0	TEST output of video system			
138	TESTOUT3					
139	TESTOUT2					
140	OVSS3X8	-	ppend GND			
141	OVDD3X5	-	Append interface VDD: 3.3V			
142	TESTOUT1	0	TEST output of video system			
143	TESTOUT0	0	TEST output of video system Output 15Hz /12.5Hz that performed VCLK dividing with TESTMODE=Oh.			
144	TESTMD3		TEST output colorion of video quetom (Normally, use for CND.)			
145	TESTMD2	 	TEST output selection of video system (Normally, use for GND.)			
146	VSS	-	GND			
147	VDDI	-	Internal VDD: 2.5V			
148	TESTMD1		TEST output colorion of video system (Normally, use for CND.)			
149	TESTMD0	_'	TEST output selection of video system (Normally, use for GND.)			
150	I-H-AV	I				
151	I-V-AV	I	Connect to GND			
152	I-F-AV	I				
153	VDDE	-	Interface VDD: 3.3V			
154	OVSS3X9	_	Append GND			
155	MCLK	I	MCLK input Perform data capture and 656 data output of the DVD decoder with this clock.			
156	I-PDINAV7					
157	I-PDINAV6		Input the video decode output of DVD (AV) DECODER			
158	I-PDINAV5] '	CCIR656 (8bit, 27MHz) input			
	I-PDINAV4					
160	VSS	_	GND			

• Pin Function (5/7)

No.	Pin Name	I/O	Pin Function				
161	OVDD3X6	-	Append interface VDD: 3.3V				
162	I-PDINAV3						
163	I-PDINAV2	1.	Input the video decode output of DVD (AV) DECODER				
164	I-PDINAV1	- I	CIR656 (8bit, 27MHz) input				
165	I-PDINAV0	-					
166	PLL-S	ı	PLL RESET input Input a RESET signal.				
167	OVSS3X10	T -	Append GND				
168	VDDE	T -	Interface VDD: 3.3V				
169	XTCK	ı	Internal SCAN and Memory SCAN (JTAG) (Normally, use for VDD.)				
170	N.C.	-	Not used				
171	VPD	ı	Electrostatic discharge prevention terminal Connect to GND.				
172	N.C.	T -	Not used				
173	SDCLKIN	ı	81MHz input for SDRAM I/F Input a pin 223 output.				
174	VSS	T -	GND				
175	VDDI	-	Internal VDD: 2.5V				
176	TRST	I					
177	TDI	ı	Dougland CCAN (ITAC) If these pine are not used use for VDD or are				
178	TMS	I	Boundary SCAN (JTAG) If these pins are not used, use for VDD or open.				
179	TCK	ı					
180	OVSS3X11	-	Append GND				
181	OVDD3X7	-	Append interface VDD: 3.3V				
182	TDO	0	Boundary SCAN (JTAG) If these pins are not used, use for VDD or open.				
183	SDDATA15						
184	SDDATA14	1,0	CDDAM DATA IN/OUT				
185	SDDATA13	1/0	SDRAM DATA IN/OUT				
186	SDDATA12						
187	VSS	-	GND				
188	VDDI	-	Internal VDD: 2.5V				
189	SDDATA11	1/0	SDRAM DATA IN/OUT				
190	SDDATA10] "//	SDRAW DATA IIVOUT				
191	OVSSX12	-	Append GND				
192	OVDD3X8	-	Append interface VDD: 3.3V				
	SDDATA9						
194	SDDATA8						
195	SDDATA7						
196	SDDATA6	I/O	SDRAM DATA IN/OUT				
197	SDDATA5						
198	SDDATA4						
199	SDDATA3						
200	VSS	_	GND				

• Pin Function (6/7)

No.	Pin Name	I/O	Pin Function
201	OVDD3X9	_	Append interface VDD: 3.3V
202	VDDI	_	Internal VDD: 2.5V
203	SDDATA2		
204	SDDATA1	I/O	SDRAM DATA IN/OUT
205	SDDATA0		
206	O-DQM3	0	SDRAM Input Mask/Output Enable 3 output
207	VDDI	-	Internal VDD: 2.5V
208	OVSS13	0	Append GND
209	O-DQM2		SDRAM Input Mask/Output Enable 2 output
210	O-DQM1	0	SDRAM Input Mask/Output Enable 1 output
211	O-DQM0		SDRAM Input Mask/Output Enable 0 output
212	VSS	_	GND
213	VDDE	_	Interface VDD: 3.3V
214	O-BA1		SDRAM Bank Select 1 output
215	O-BA0	0	SDRAM Bank Select 0 output
216	O-XCS-DRAM	0	SDRAM Chip Select
217	O-CKE	0	SDRAM Clock Enable output
218	OVSSX14	_	Append GND
219	OVDD3X10	_	Append interface VDD: 3.3V
220	O-XWE	0	SDRAM Write Enable output
221	O-XRAS	0	SDRAM Row Address Strobe output
222	O-XCAS	0	SDRAM Column Address Strobe output
223	SDCLK	0	81MHz PLL output for SDRAM Input to CLK pin of SDRAM and pin 173 of this LSI.
224	VSS	_	GND
225	VDDE	_	Interface VDD: 3.3V
226	O-SDADDRESS10		
227	O-SDADDRESS9	0	SDRAM ADDRESS output
228	O-SDADDRESS8		SUNAIN ADDICESS output
229	O-SDADDRESS7		
230	OVDD3X11	_	Append interface VDD: 3.3V
231	OVSS3X15	-	Append GND
232	O-SDADDRESS6		
	O-SDADDRESS5	0	SDRAM ADDRESS output
234	O-SDADDRESS4		Solve in Abortago output
235	O-SDADDRESS3		
236	VSS	-	GND
237	VDDE	-	Interface VDD: 3.3V
238	O-SDADDRESS2		
239	O-SDADDRESS1	0	SDRAM ADDRESS output
240	O-SDADDRESS0		

DVR-7000

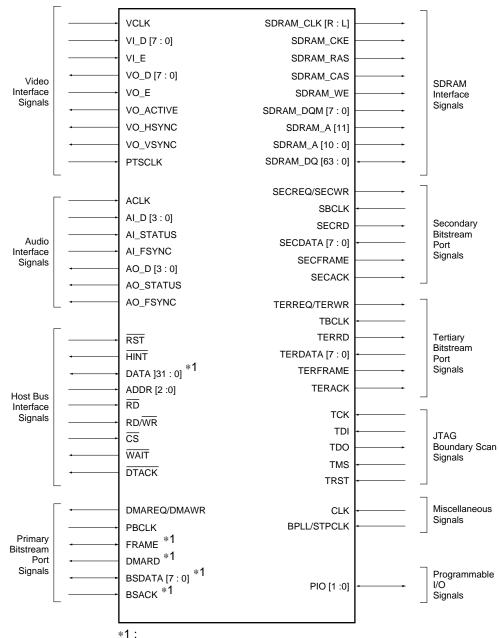
• Pin Function (7/7)

No.	Pin Name	I/O	Pin Function
241	SDDATA31	I/O	SDRAM DATA IN/OUT
242	VDDI	-	Internal VDD: 2.5V
243	OVSSX16	_	Append GND
244	SDDATA30		
245	SDDATA29	I/O	SDRAM DATA IN/OUT
246	SDDATA28		
247	VSS	_	GND
248	OVDD3X12	_	Append interface VDD: 3.3V
249	VDDI	_	Internal VDD: 2.5V
250	SDDATA27		
251	SDDATA26		
252	SDDATA25	I/O	SDRAM DATA IN/OUT
253	SDDATA24		
254	SDDATA23		
255	OVSSX17	_	Append GND
256	OVDDX13	-	Append interface VDD: 3.3V

■ DVXCEL-BA1 (MAIN ASSY: IC5005)

• MPEG2 Video Codec

Block Diagram



Note that BSDATA [7:0] share pins with DATA [28:21], BSACK shares a pin with DATA [31], FRAME shares a pin with DATA [30], and DMARD shares a pin with DATA [29].

• Pin Function

Mark	Pin Name	I/O	Pin Function
Host Bus I/F	•		
XRST	Y19	I	Chip Reset
XHINT	V17	0	Host Interrupt Request
DATA [31 : 16]	V5, W4, Y3, V6, W5, Y5, V7, W6, Y6, W7, V8, Y7, W8, V9, Y8, W9	I/O TS	32-bit host interface data bus upper 16 bits. Upper 11 bits shared with BSACK (Data[31]), FRAME (Data[30]), DMARD (Data[29]) and BSData[7:0](Data[28:21]) pins.
DATA [15 : 0]	Y9, V10, W10, Y10, Y11, W11, Y12, W12, V11, Y13, V12, W13, Y14, W14, Y15, V14	I/O TS	Lower 16 bits host interface data bus
ADDR [2:0]	V16, Y18, W15	I	Host Address bus (16-bit word address)
XRD	Y16	ı	Host I-mode Write strobe/M-mode direction signal
xcs	V15	I	Host Chip Select
XWAIT	W18	0	Host Ready
XDTACK	W17	0	Host Data Transfer Acknowledge
Primary Bitstream I/F	!		
DMAREQ/DMAWR	Y17	0	Host DMA or Primary Bitstream port transfer request or write transfer request
PBCLK	Y4	ı	Separate Primary Bitstream port clock, 0 - 27 MHz
FRAME	W4	I/O TS	Separate Primary Bitstream start of packet
DMARD	Y3	0	Separate Primary Bitstream port, outgoing transfer
BSDATA [7:0]	V6, W5, Y5, V7, W6, Y6, W7, V8	I/O TS	Separate bitstream port data
BSACK	V5	ı	Separate bitstream transfer grant
Secondary Bitstream	l/F		
SBCLK	Y1	I	Secondary bitstream port clock, 0 - 27 MHz
SECRD	U1	0	Secondary bitstream port, outgoing transfers
SECDATA [7:0]	T3, U2, W2, V3, U3, V4, W3, Y2	I/O TS	Secondary bitstream port data
SECFRAME	V2	I/O TS	Secondary bitstream start of packet frame
SECACK	W1	ı	Secondary bitstream transfer grant
SECREQ/SECWR	V1	0	Secondary bitstream port transfer or write transfer request
Tertiary Bitstream I/F			
TBCLK	L1	I	Tertiary bitstream port clock, 0 -27 MHz
TERRD	G2	0	Tertiary bitstream port, outgoing transfers
TERDDATA [7:0]	J2, J1, K2, K1, L2, K3, L3, M2	I/O TS	Tertiary bitstream port data
TERFRAME	H1	I/O TS	Tertiary bitstream start of packet frame
TERRACK	H2	Ī	Tertiary bitstream transfer grant
TERREQ/TERWR	G1	0	Tertiary bitstream port transfer or write transfer request

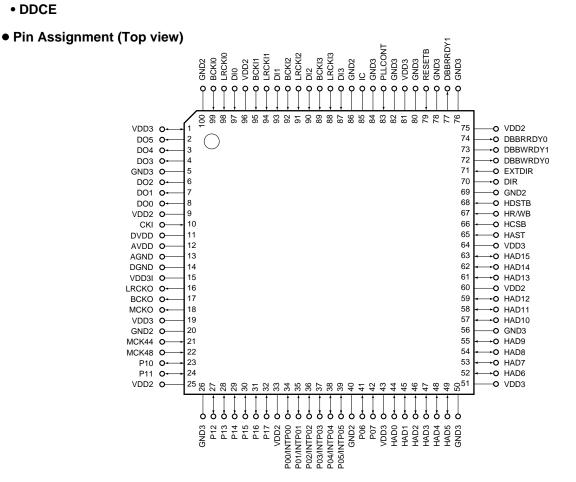
Mark	Pin Name	I/O	Pin Function
Video I/F	!		
PTSCLK	M1	I	Video PTS Clock. This required clock is timing reference for the internal presentation timestamp (PTS) counter. The external PTS clock frequency is either 27 MHz or 90 kHz. The internal frequency is 90 kHz. Microcode autodetects the PTS clock frequency and adjusts its internal divider appropriately. PTSCLK is asynchronous to all other processor clocks. C-Cube recommends that your board include parallel AC termination or DC termination to terminate this clock's source driver.
VCLK	T20	ı	Video Clock. VCLK is the video input/output sampling clock. Input data is sampled and output data is driven on the rising edge of VCLK. Valid VCLK frequencies are 27 MHz and 54 MHz. VCLK is asynchronous to all other processor clocks.
VI_D [9 : 0]	M20, M19, M18, N20, N19, P20, N18, P19, R20, R18	ı	Video input Data. These pins capture the interleaved luma and chroma samples (4:2:0 format). Micro-code determines whether the data order is (Cb, Y, Cr, Y) or (Y, Cb, Y, Cr). The DVxcel processor decodes the SAV codes in the incoming video data to determine whether the video is active and whether the field is odd or even. For 8-bit input, drive data onto pins VI_D [9:2] and ground pins VI_D [1:0].
VI_E	P18	ı	Video Input Enable. When VI_E is asserted, the DVxcel processor samples input pels on the VI_D bus and increments the horizontal position counter. This signal allows external downsampling hardware to throttle video capture without generating a nonstandard video clock.
VO_ACTIVE	R19	O TS VC	Video Output Active. The DVxcel processor asserts VO_ACTIVE when an active (nonblanked) pel is present on the VO_D bus.
VO_D [7:0]	U19, V20, T19, V19, W20, W19, U18, Y20	O TS VC	Video Output Data. The DVxcel processor outputs interleaved luma and chroma samples (4 : 2 : 0 format) on these pins. Microcode detemines whether the data order is either (Cb, Y, Cr, Y) or (Y, Cb, Y, Cr). The DVxcel processor inserts an SAV code with the appropriate V and F bits into the output stream starting four clocks before VO_ACTIVE is asserted. The V bit in the SAV code is set to one during vertical blanking. The F bit is set to one when the current field is even. The DVxcel processor inserts an EAV code into the output stream starting on the clock that VO_ACTIVE is deasserted.
VO_E	V18	I	Video Output Enable. When VO_E is asserted, the output value and horizontal position are held to the same value as in the previous clock, if the video output was not blanked during that clock. VO_E allows external hardware to throttle video output without generating a nonstandard video clock. VO_E is ignored with echo active. VO_E can be used with genlock or video capture active as long as the time to transfer the last active pel is less than the total input frame time.
VO_HSYNC	U20	O TS VC	Video Horizontal Synchronization. The DVxcel processor asserts VO_HSYNC at the first pel in each line for the duration specified by the microcode. Note that the polarity of this output is programmable via the OSPOL bit in the Video Control Register.
VO_VSYNC	T18	O TS VC	Video Vertical Synchronization. The DVxcel processor asserts VO_VSYNC at the beginning of an odd field and holds it assrted for the number of lines specified by the microcode. For interlaced transfer, the processor asserts VO_VSYNC starting in the middle of the last scan line of an odd field. VO_VSYNC is then deasserted in the middle of the scan line after the number of lines specified by the microcode (next even field). Note that the polarity of this output is programmable via the OSPOL bit in the Video Control Register.

Mark	Pin Name	I/O	Pin Function	
SDRAM I/F				
XSDRAM_CAS	B12	0	SDRAM Column Address Strobe.	
XSDRAM_RAS	C12	0	SDRAM Row Address Strobe.	
SDRAM_A [11]	B8	0	SDRAM Bank Address This output determines which SDRAM bank is selected.	
SDRAM_A [10 : 0]	A8, C9, B9, A9, C10, B10, A10, A11, B11, C11, A12	0	SDRAM Address	
SDRAM_CLK [R :L]	A13, B7	0	SDRAM Clock. These outputs are buffered versions of the internal processor clock. SDRAM_CLKR and SDRAM_CLKL are identical. Two outputs are provided to reduce the output loading and simplify PCB layout.	
SDRAM_CKE	B13	0	SDRAM Clock Enable.	
XSDRAM_WE	C13	0	SDRAM Write Enable.	
SDRAM_DQM [7 : 0]	A6, C7, A7, C8, A14, B14, A15, C14	0	SDRAM Data Mask (Byte Enables). These bits connect directly to the appropriate UDQM/LDQM inputs. SDRAM_DQM0 controls the most-significant byte; SDRAM_DQM7 controls the least-significant byte. They are used for partial stores and termination of burst write transfers.	
SDRAM_DQ [63 : 0]	F20, G20, F19, E20, F18, E19, D20, D19, G17, C20, B20, E18, C19, D18, A20, E17, C18, D17, A19, B19, C17, D16, A18, B18, B17, C16, D15, A17, B16, C15, A16, B15, B6, C6, A5, B5, A4, C5, D6, A3, B4, B3, A2, C4, D5, E4, C3, B2, A1, F4, B1, D3, C2, E3, G4, D2, C1, D1, F3, E2, E1, F2, G3, F1	I/O TS	SDRAM Data.	
Audio I/F	•			
ACLK	N1	I	Audio Clock. ACLK is the serial clock used for audio input and output. Input data is sampled on and output data is driven on the active edge of ACLK. Microcode determines whether the active edge is the rising or the falling edge. ACLK is asynchronous to all other DVxcel processor clocks. Its maximum frequency is 9.09 MHz. The frequency of ACLK and the number of clocks per sample depend on the audio frame format selected.	
AI_D [3 : 0]	P1, M3, N2, N3	I	Audio Input Data. Up to eight channels of serial audio data are clocked into the AI_D [3:0] pins. With two samples per frame, channels 2n and (2n + 1) use pin AI_Dn. With one sample per frame, channel n uses pin AI_Dn. Microcode determines the number of samples per frame. The processor samples AI_D [3:0] on the active edge of ACLK.	
AI_FSYNC	P2	I	Audio Frame Sync In. Asserting AI_FSYNC indicates the start or end of the next input sample or frame as specified by the selected audio frame format (Section 9.2). The processor samples AI_FSYNC on the active edge of ACLK.	
AI_STATUS	P3	I	Audio Input Status. Audio status information (32 bits for each sample frame) is clocked in on the active edge of ACLK.	
AO_D [3:0]	R3, T2, R1, R2	0	Audio Output Data. The DVxcel processor clocks up to eight channels of serial audio data from the four AO_D outputs. With two samples per frame, channels 2n and (2n + 1) use pin AO_Dn. With one sample per frame, channel n uses pin AO_Dn. Microcode determines the number of samples per fram. AO_D [3:0] are driven on the active edge of ACLK.	
AO_FSYNC	T1	0	Audio Frame Sync Out. The DVxcel processor asserts AO_FSYNC as an indicator of the start or end of the next output sample or frame as specified by the selected audio frame format.	
AO_STATUS	R4	0	Audio Output Status. Audio status information (32 bits for each sample frame) is clocked out of the DVxcel processor on the active edge of ACLK.	

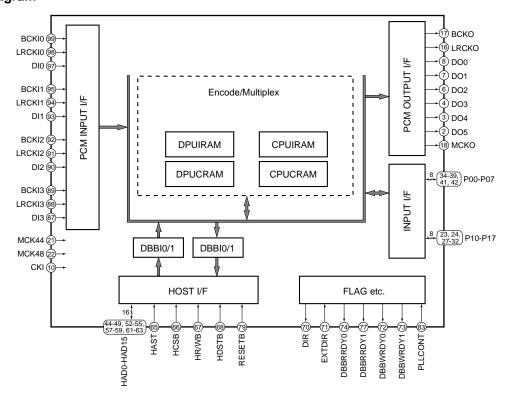
Mark	Pin Name	I/O	Pin Function
JTAG Boundary Sca	n I/F		
тск	K20	I	JTAG Test Clock. This input clocks state information, boundary scan instructions, and test data into and out of the DVxcel processsor during Test Access Port (TAP) operation.
TDI	K18	I	JTAG Test Data In. Test data and test instructions are shifted serially into this input during TAP operation.
TDO	L19	O TS	JTAG Test Data Out. Test data and test instructions are shifted serially out of this output during TAP operation.
TMS	L18	I PUP	JTAG Test Mode Select. This input controls the state of the DVxcel processor's TAP controller.
XTRST	K19	I PUP	JTAG Test Reset. Asynchronously asserting this input causes the DVxcel processor to initialize the TAP controller. If the JTAG port is not used, tie this input LOW. Otherwise, pull it down with a 470 Ω resistor.
Miscellaneous			
BPLL/STPCLK	H20	I	Bypass PLL/Stop Clock. A LOW on this input selects PLL/2 output to drive the internal processor clock, and a HIGH selects the CLK input pin to drive the internal processor clock. The selecet value is latched on the deassertion of XRST and is used until the DVxcel processor is externally reset again. For normal system operation, tie this input LOW to select the PLL/2 output.
CLK	J20	I	Internal Clock Reference. The internal processor clock uses this input as the timing reference. CLK is normally 27.5 MHz. It is internally multiplied by 8 and divided by 2 to yield the 110 MHz internal clock C-Cube recommends that your board include parallel AC termination or DC termination to terminate this clock's source driver.
Programmed I/O			
PIO [1 : 0]	J3, H3	I/O	Programmed I/O. These pins are individually programmed as inputs or outputs through the Programmed I/O Register. 4.7 k Ω pullup resistors should be connected to +3.3V.
Power, Ground and I	No Connect	•	
C_V	H18	0	Clock VCO Control Voltage, used for testing purposes. Leave open (NC).
VDD	D7-D14, E9-E12, J5, J16, K5, K16, L5, L16, M5, M16, T9-T12, U7-U14	_	3.3V Digital Power. These pins are the primary power supply for the input and output voltages of non-host interface pads.
VDD_A	G18	-	3.3V Analog Power for the Internal Clock PLL. This pin provides the analog power for the DVxcel processor's internal clock phase locked loop.
VDDQ	D4, F17, H4, H17, J4, J17, K4, L17, M4, N4, N17, P4, P17, T17	_	1.9V Digital Power. These pins supply power to the core. They have been separated from the standard power supply pins so that you can add extra decoupling, if needed.
VDD_P	G19	_	3.3V Digital Power for the Internal Clock PLL. This pin provides digital power to the DVxcel processor's internal clock phase locked loop. Connect it to the system power plane.
GND	H8-H13, J8-J13, K8-K13, L8-L13, M8-M13,N8-N13	_	Digital Ground. These pins are the primary ground pins for the logic on the DVxcel processor.
GND_A	J18	_	Analog Ground for the Internal Clock PLL. This pin provides the analog ground for the DVxcel processor's internal clock phase locked loop.
GND_P	H19	_	Digital Ground for the Internal Clock PLL. This pin provides ground to the DVxcel processor's internal clock phase locked loop. Connect it to the system ground plane.
NC	J19, K17, L4, L20, M17, R17, T4, U4-U6, U15-U17, V13	_	No Connect.

■ UPD61003 (MAIN ASSY: IC6002)

• DDCE



Block Diagram



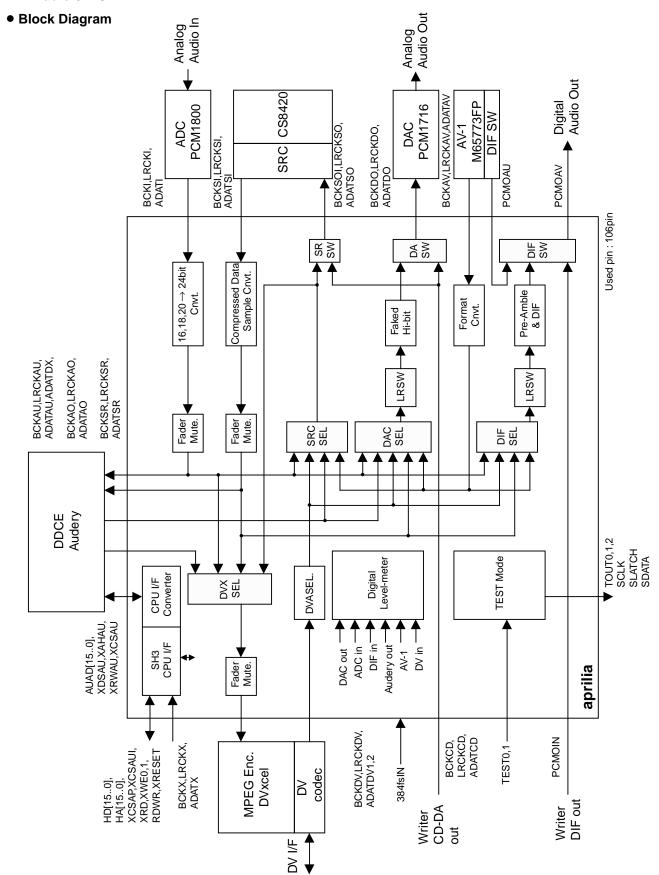
• Pin Function

VIDOS UP 4.39 y power supply	No.	Pin Name	I/O	Pin Function		
3 DO4 O PCM output data 3	1	VDD3	I/O			
3 DO4 O PCM output data 3	2	DO5				
Cost	3	DO4	0	'		
5 GND3	4	DO3		PCM output data 3		
7	5	GND3	_	Ground (3.3V)		
8 OOO PCM output data 0 PCM output 0 PCM outp	6	DO2		PCM output data 2		
9 VDQ2	7	DO1	0	PCM output data 1		
10 Ckl Viv Viv	8	DO0		PCM output data 0		
11	9	VDD2	_	+2.5V power supply		
13 ASND	10	СКІ	I	System clock input		
AGND	11	DVDD	-	+2.5V power supply (for divider of internal PLL circuit)		
14	12	AVDD	_	+2.5V power supply (for analog circuit of internal PLL circuit)		
15	13	AGND	_	Ground (for analog circuit of internal PLL circuit)		
16 LRCKO O Common LRCK for PCM output 0 through 5	14	DGND	_	Ground (for digital circuit of internal PLL circuit)		
17	15	VDD3I	_	+3.3V power supply		
No	16	LRCKO	0	Common LRCK for PCM output 0 through 5		
VDD3	17	ВСКО	0	Common bit clock for PCM output 0 through 5		
19 VDD3	18	мско	0	Audio master clock output Output 256fs or 384fs in accordance with the setting of the PCM mode register.		
MCK44	19	VDD3	_			
Input 256ts or 384fs in accordance with the setting of the PCM mode register.	20	GND2	_	Ground (2.5V)		
Input 250s of 348t in accordance with the setting of the PCM mode register.	21	MCK44	ı	Audio master clock input (for 44.1kHz)		
Input 256/is or 384/is in accordance with the setting of the PCM mode register.	21	WCK44	'			
Vo If any of these pins are connected to a high impedance (1MΩ min.), pull it down or up with a resistance of 1kΩ or higher. Vo Volume	22	MCK48	I	Input 256fs or 384fs in accordance with the setting of the PCM mode register.		
A	23	P10	.,,			
26 GND3			1/0	higher.		
27 P12			_	1 117		
P13			-	Ground (3.3V)		
P14						
First Fir				General-nurnose I/O norts		
P16 32 P17 P16 P17 P17 P18 P18 P19 P19			I/O	' ' ' '		
32 P17				higher.		
33 VDD2						
Pool/INTP00 35 Po1/INTP01 36 Po2/INTP02 37 Po3/INTP03 38 Po4/INTP04 39 Po5/INTP05 40 GND2 For a position of the p						
POI/INTPO1 36 PO2/INTP02 37 PO3/INTP03 38 PO4/INTP04 39 PO5/INTP05 40 GND2 41 PO6 42 PO7 PO7			_	+2.5V power supply		
Second (2.5V) Second (2.5						
37 P03/INTP03 38 P04/INTP04 39 P05/INTP05	L		I/O			
Section of the property of						
39 P05/INTP05			ı			
40 GND2 - Ground (2.5V) 41 P06 HO 42 P07 I/O If any of these pins are connected to a high impedance (1MΩ min.), pull it down or up with a resistance of 1kΩ or higher. 43 VDD3 - +3.3V power supply 44 HAD0 +5 HAD1 45 HAD1 HAD3 46 HAD2 HOst address/data bus 47 HAD3 HAD4 49 HAD5 HAD5						
41P06I/OGeneral-purpose I/O ports If any of these pins are connected to a high impedance (1MΩ min.), pull it down or up with a resistance of 1kΩ or higher.43VDD3-+3.3V power supply44HAD0+3.3V power supply45HAD1+46HAD247HAD3+48HAD449HAD5 General-purpose I/O ports If any of these pins are connected to a high impedance (1MΩ min.), pull it down or up with a resistance of 1kΩ or higher. +3.3V power supply Host address/data bus				Ground (2.5V)		
1/O If any of these pins are connected to a high impedance (1MΩ min.), pull it down or up with a resistance of 1kΩ or higher. 43 VDD3			_	·		
43 VDD3 - +3.3V power supply 44 HAD0 45 HAD1 46 HAD2 47 HAD3 48 HAD4 49 HAD5			I/O	If any of these pins are connected to a high impedance (1M Ω min.), pull it down or up with a resistance of 1k Ω or		
44 HAD0 45 HAD1 46 HAD2 47 HAD3 48 HAD4 49 HAD5	43		_			
45 HAD1 46 HAD2 47 HAD3 48 HAD4 49 HAD5						
46 HAD2 47 HAD3 48 HAD4 49 HAD5						
47 HAD3						
48 HAD4 49 HAD5	<u> </u>		I/O	Host address/data bus		
49 HAD5						
			_	Ground (3.3V)		

No.	Pin Name	1/0	Pin Function
51	VDD3	_	+3.3V power supply
52	HAD6		The state of the s
53	HAD7		
54	HAD8	I/O	Host address/data bus
55	HAD9		
56	GND3	_	Ground (3.3V)
57	HAD10		
58	HAD11	1/0	Host address/data bus
59	HAD12	.,,	11001 addi 000/data 240
60	VDD2	_	+2.5V power supply
61	HAD13		12.57 porter suppry
62	HAD14	1/0	Host address/data bus
63	HAD15	., 0	1.1601 444.1605, 4414 240
	VDD3	_	+3.3V power supply
65	HAST	1	Host address strobe
	HCSB	· 	Chip select
67	HR/WB	· ·	Host read/write status
68	HDSTB	i	Host data strobe
69	GND2	_	Ground (2.5V)
00	ONDZ		HAD bus drive controll flag output This flag indicates the bus driving direction of HAD15 through HAD0.
70	DIR	0	"H": output, "L": input
71	EXTDIR	ı	HAD bus drive control flag This pin controls the bus drive control flag from DIR. Connect this pin to GND.
70	DDDWDDVO		DBBI0 write ready flag
72	DBBWRDY0	0	Writing is enabled when this flag is high and disabled when it is low.
73	DBBWRDY1		DBBI1 write ready flag This flag enables write access to the DBBI1 resistor. Writing is enabled when this flag is high and disabled when it is low.
74	DBBRRDY0	0	DBBO0 read ready flag This flag enables read access to the DBBO0 resistor. Reading is enabled when this flag is high and disabled when it is low.
75	VDD2	_	+2.5V power supply
76	GND3	_	Ground (3.3V)
77	DBBRRDY1	0	DBBO1 read ready flag This flag enables read access to the DBBO1 resistor. Reading is enabled when this flag is high and disabled when it is low.
78	GND3	_	Ground (3.3V)
79	RESETB	ı	System reset
80	GND3	_	Ground (3.3V)
81	VDD3	_	+3.3V power supply
82	GND3	_	Ground (3.3V)
83	PLLCONT	ı	PLL operation mode If this pin is connected to GND (PLL mode), the internal operating clock frequency is two times higher than of the clock input to the CKI pin. If it is connected to DVDD3 (direct mode), the internal operating clock frequency is equal to that of the clock input to the CKI pin. Usually, use the PLL mode by connecting this pin to GND.
84	GND3	_	Ground (3.3V)
85	IC	_	Open
86	GND2	_	Ground (2.5V)
87	DI3	I	PCM input data 3
	LRCKI3	ı	LRCK for PCM input 3
	BCKI3	ı	Bit clock for PCM input 3
	DI2	ı	PCM input data 2
91	LRCKI2	ı	LRCK for PCM input 2
	BCKI2	I	Bit clock for PCM input 2
93	DI1	ı	PCM input data 1
94	LRCKI1	ı	LRCK for PCM input 1
	BCKI1	ı	Bit clock for PCM input 1
96	VDD2	_	+2.5V power supply
97	DIO	ı	PCM input data 0
	LRCKI0	ı	LRCK for PCM input 0
99	BCKI0	ı	Bit clock for PCM input 0
	GND2	_	Ground (2.5V)
	L		· '

■ PE7004A (MAIN ASSY: IC6003)

• Audio I/F IC



• Pin Function (1/2)

1 VDD	No.	Pin Name	I/O	Pin Function		Pin Name	I/O	Pin Function	
3 TOO	1	VDD	_	VDD	49	HA10			
1	2	TMS	-		50	HA9	1	CPU I/F Address	
S TESTO 1 TEST1	3	TDO	_	JTAG	51	HA8			
First	4	TRST	_		52	GND	-	GND	
Section Color Co	5	TEST0			53	VDD	-	VDD	
B TOUT1 3 TOUT2 10 SCLK 57 HA4 58 HA3 59 HA2 60 HA1 60 H	6	TEST1	'		54	HA7			
9 TOUT2	7	TOUT0			55	HA6			
9 TOUT2 10 SCLK 11 SDATA 12 SLATCH 13 GND	8	TOUT1		TEOT	56	HA5			
10 SCLK 58 HA3 59 HA2 60 HA1 70 70 MD 62 MD 70 MD MD 70 MD MD MD MD MD MD MD M	9	TOUT2		IESI	57	HA4	١.	CDLLI/E Address	
12 SLATCH	10	SCLK			58	HA3	'	CPU I/F Address	
13 GND	11	SDATA			59	HA2			
14	12	SLATCH			60	HA1			
15 PCMOIN 16 LRCKCD 16 LRCKCD 17 BCKCD 18 Audio signal LRCK from the drive 64 HD15 Audio signal DATA from the drive 66 HD13 Audio signal DATA from the drive 66 HD13 Audio signal DATA from the drive 66 HD13 Audio signal DATA to the Dvxcel 67 HD12 Audio signal DATA to the Dvxcel 68 HD11 Audio signal DATA to the Dvxcel 69 HD10 Audio signal DATA from the Dvxcel 70 HD9 Audio signal DATA from the Dvxcel 71 HD8 Audio signal DATA from the Dvxcel 72 GND — GND Audio signal DATA from the Dvxcel 73 VDD — VDD 75 HD6 Audio signal DATA from the Dvxcel 74 HD7 Audio signal DATA from the Dvxcel 75 HD6 Audio signal DATA from the Dvxcel 76 HD5 Audio signal DATA from the AV1 76 HD6 Audio signal DATA from the AV1 77 HD4 Audio signal BCK from the AV1 78 HD3 Audio signal BCK from the AV1 79 HD2 Audio sign	13	GND	_	GND	61	HA0			
16 LRCKCD 1	14	VDD	_	VDD	62	GND	_	GND	
17 BCKCD	15	PCMOIN		ADIF from the drive	63	VDD	_	VDD	
17 BCKCD	16	LRCKCD		Audio signal LRCK from the drive	64	HD15			
19	17	BCKCD	ı	Audio signal BCK from the drive	65	HD14			
20 BCKX	18	ADATCD		Audio signal DATA from the drive	66	HD13			
20 BCKX	19	LRCKX		Audio signal LRCK to the Dvxcel	67	HD12	.,_	CPU I/F Data	
22 LRCKDV	20	BCKX	0	Audio signal BCK to the Dvxcel	68	HD11	1/0		
23 BCKDV	21	ADATX		Audio signal DATA to the Dvxcel	69	HD10			
Addio signal DATA from the Dvxcel 72 GND	22	LRCKDV		Audio signal LRCK from the Dvxcel	70	HD9			
Audio signal DATA from the Dvxcel 72 GND - GND	23	BCKDV		Audio signal BCK from the Dvxcel	71	HD8			
26 GND	24	ADATDV1	l	_	72	GND	_	GND	
26 GND	25	ADATDV2		Audio signal DATA from the Dvxcel	73	VDD	_	VDD	
Audio signal LRCK from the AV1 76 HD5	26	GND	_		74	HD7			
Audio signal BCK from the AV1 77 HD4	27	VDD	_	VDD	75	HD6			
Audio signal BCK from the AV1 77 HD4	28	LRCKAV		Audio signal LRCK from the AV1	76	HD5			
30 ADATAV	29	BCKAV	ı		77	HD4	.,,		
32 XRESET 1 Chip reset 80 HD1	30	ADATAV		Audio signal DATA from the AV1	78	HD3	1/0	CPU I/F Data	
33 XCSAUI 34 XCSAP 35 RDWR 25 RDWR 36 GND - GND - GND - VDD - VDD	31	PCMOAV	0	ADIF output	79	HD2			
Aprilia CS	32	XRESET		Chip reset	80	HD1			
Aprilia CS	33	XCSAUI		CS to Audery	81	HD0			
36 GND	34	XCSAP	l	Aprilia CS	82	GND	_	GND	
37 VDD	35	RDWR		CPU I/F RDWR	83	VDD	_	VDD	
CLK for CPU I/F 86 AUAD13 1 CPU I/F WR L byte 87 AUAD12 Audery Bus AUAD13 Audery Bus AUAD14 Audery Bus AUAD15 Audery Bus AUAD16 Audery Bus AUAD16 Audery Bus AUAD17 Audery Bus AUAD18 Audery Bus AUAD10 Audery Bus AUAD10 Audery Bus AUAD10 Audery Bus AUAD10 AU	36	GND	_	GND	84	AUAD15			
39 XWRL 1	37	VDD	_	VDD	85	AUAD14			
Audery Bus Audery Bus Audery Bus Audery Bus Audery Bus	38	CLK40M		CLK for CPU I/F	86	AUAD13			
Audery Bus Audery Bus Audery Bus Audery Bus Audery Bus	39	XWRL			87	AUAD12		Auden Bus	
41 XRD CPU I/F RD 89 AUAD10 42 GND - GND 90 AUAD9 43 VDD - VDD 91 AUAD8 44 HA15 92 GND - GND 45 HA14 93 VDD - VDD 46 HA13 I CPU I/F Address 94 AUAD7 47 HA12 I/O Audery Bus	40	XWRH		CPU I/F WR H byte			1/0	Audery Bus	
42 GND - GND 90 AUAD9 43 VDD - VDD 91 AUAD8 44 HA15 92 GND - GND 45 HA14 93 VDD - VDD 46 HA13 I CPU I/F Address 94 AUAD7 47 HA12 95 AUAD6 I/O Audery Bus	41	XRD		CPU I/F RD					
43 VDD - VDD 91 AUAD8 - GND 44 HA15 92 GND - GND 45 HA14 93 VDD - VDD 46 HA13 I CPU I/F Address 94 AUAD7 AUAD6 I/O Audery Bus	42	GND	_	GND					
44 HA15 45 HA14 46 HA13 47 HA12 92 GND - 93 VDD - 94 AUAD7 95 AUAD6 I/O Audery Bus	43	VDD	_	VDD					
45 HA14 46 HA13 47 HA12 93 VDD 94 AUAD7 95 AUAD6 I/O Audery Bus	44	HA15					_	GND	
46 HA13 I CPU I/F Address 94 AUAD7 47 HA12 95 AUAD6 I/O Audery Bus							_	VDD	
47 HA12 95 AUAD6 I/O Audery Bus			ı	CPU I/F Address	94				
	47	HA12					1/0	Audery Bus	
	48	HA11			96	AUAD5	1		

• Pin Function (2/2)

No.	Pin Name	I/O	Pin Function								
97	AUAD4										
98	AUAD3	1									
99	AUAD2	I/O	Audery Bus								
100	AUAD1										
101	AUAD0		GND								
102	GND	-	GND								
103	VDD	-	VDD								
104	XAHAU		Address hold signal of Audery								
105	XDSAU		Data hold signal of Audery								
106	XRWAU	0	Audery RW								
107	XCSAU	1	Audery CS								
108	GND	-	GND								
109	VDD	-	VDD								
110	LRCKAU		Audio signal LRCK from the Audery								
111	BCKAU		Audio signal BCK from the Audery								
112	ADATAU	ı	Audio signal DATA from the Audery								
113	ADATDX	İ	Audio signal DATA from the Audery								
114	PCMOAU	İ	ADIF signal from the AV1								
115	LRCKSR		Audio signal LRCK to the Audery								
116	BCKSR		Audio signal BCK to the Audery								
117	ADATSR		Audio signal DATA to the Audery								
118	LRCKAO	0	Audio signal LRCK to the Audery								
119	BCKAO		Audio signal BCK to the Audery								
120	ADATAO		Audio signal DATA to the Audery								
121	GND	-	GND								
122	VDD	-	VDD								
123	CLK36M	I	CLK for Audio system circuit								
124	LRCKDO		Audio signal LRCK to the DAC								
125	BCKDO	0	Audio signal BCK to the DAC								
126	ADATDO		Audio signal DATA to the DAC								
127	LRCKI		Audio signal LRCK from the ADC								
128	BCKI	ı	Audio signal BCK from the ADC								
129	ADATI		Audio signal DATA from the ADC								
130	GND	-	GND								
_	VDD	-	VDD								
132	LRCKSI		Audio signal LRCK from the SRC								
133	BCKSI	ı	Audio signal BCK from the SRC								
134	ADATSI	L	Audio signal DATA from the SRC								
135	LRCKSO		Audio signal LRCK to the SRC								
136	BCKSO	0	Audio signal BCK to the SRC								
137	ADATSO	L	Audio signal DATA to the SRC								
138	GND	_	GND								
139	VDD	_	VDD								
140	ATPGEN	_	IC TEST								
141	SCANEN	_	IC TEST								
142	TCK	_	JTAG								
143	TDI	_	JTAG								
144	GND	-	GND								

■ CS8420-CS (MAIN ASSY: IC6004)

• Sampling Rate Converter

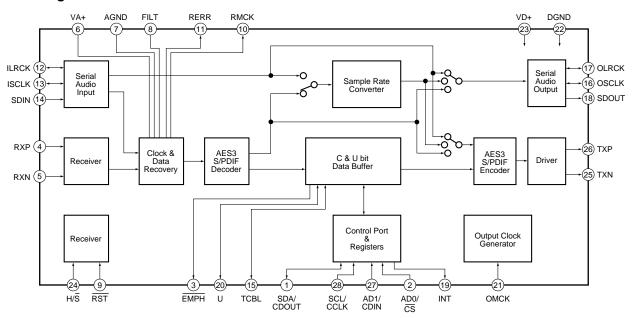
• Pin Assignment (Top view)

SDA/CDOUT □ 28 SCL/CCLK AD1/CDIN AD0/CS □ 27 26 TXP EMPH □ 25 TXN RXP [24 H/S RXN 🗆 23 VD+ 22 DGND AGND □ 21 D OMCK FILT 🗆 RST □ 20 🗖 U 19 | INT RMCK □ 10 18 SDOUT RERR □ 17 OLRCK 12 ILRCK □ 16 OSCLK ISCLK ☐ 13 SDIN 🗆 14 15 TCBL

• Pin Function

No.	Pin Name	I/O	Pin Function					
1	SDA/CDOUT	0	Serial control data I/O (I ² C) / data out (SPI)					
2	AD0/CS	I	Address bit 0 (I ² C) / Control port chip select (SPI)					
3	EMPH	0	Pre-emphasis indicator output					
4	RXP	ı	Differential line receiver inputs					
5	RXN	•	Differential line receiver inputs					
6	VA+	_	Positive analog power (+5V)					
7	AGND	_	Analog ground					
8	FILT	_	PLL loop filter					
9	RST	I	Reset input					
10	RMCK	0	Input section recovered master clock output					
11	RERR	0	Receiver error indicator					
12	ILRCK	I/O	Serial audio input port L/R clock input or output					
13	ISCLK	I/O	Serial audio input port bit clock input or output					
14	SDIN	I	Serial audio input port data input					
15	TCBL	0	Transmit channel status block start					
16	OSCLK	I/O	Serial audio output port bit clock input or output					
17	OLRCK	I/O	Serial audio output port L/R clock input or output					
18	SDOUT	0	Serial audio output port data output					
19	INT	0	Interrupt output					
20	U	0	User data					
21	OMCK	I	Outout section master clock input					
22	DGND	_	Digital ground					
23	VD+	_	Positive digital power (+5V)					
24	H/S	I	Hardware or software control mode select					
25	TXN	0	Differential line driver outpute					
26	TXP	U	Differential line driver outputs					
27	AD1/CDIN	ı	Address bit 1 (I ² C) / Control port chip select (SPI)					
28	SCL/CCLK	ı	Control port clock					

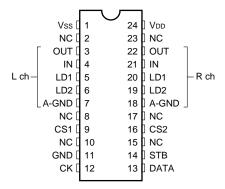
Block Diagram



■ TC9412AF (MAIN ASSY : IC8002)

• ER-VR IC

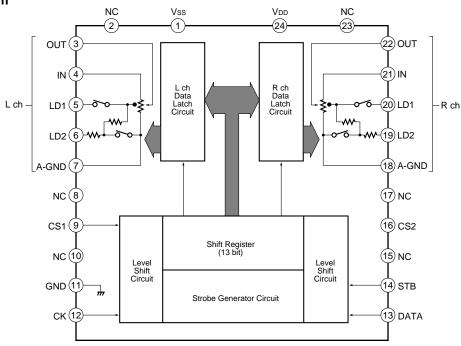
• Pin Assignment (Top view)



• Pin Function

Pin	Pin Name	Pin Function
1	Vss	Negative power supply pin
2	NC	Non connection pin
3	OUT	L ch Volume output pin
4	IN	L ch Volume input pin
5	LD1	L ch Loudness tap output pin
6	LD2	L ch Loudness tap output pin
7	A-GND	L ch Analog ground pin
8	NC	Non connection
9	CS1	Chip select input pin
10	NC	Non connection
11	GND	Digital ground pin
12	СК	Clock input pin
13	DATA	Data input pin
14	STB	Strobe input pin
15	NC	Non connection
16	CS2	Chip select input pin
17	NC	Non connection
18	A-GND	R ch Analog ground pin
19	LD2	R ch Loudness tap output pin
20	LD1	R ch Loudness tap output pin
21	IN	R ch Volume input pin
22	OUT	R ch Volume output pin
23	NC	Non connection
24	VDD	Positive power supply pin

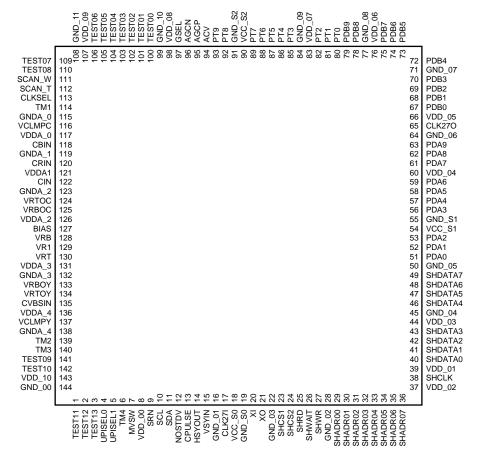
• Block Diagram



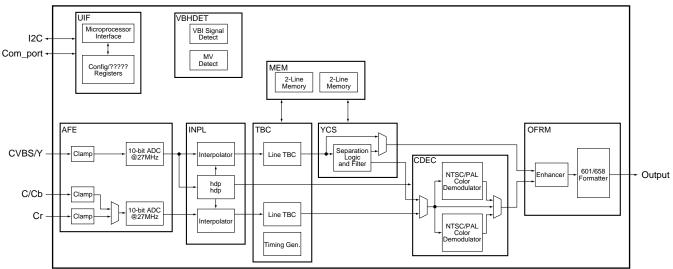
PD0272A (MAIN ASSY : IC8008)

Video Decoder IC

Pin Assignment (Top view)



Block Diagram



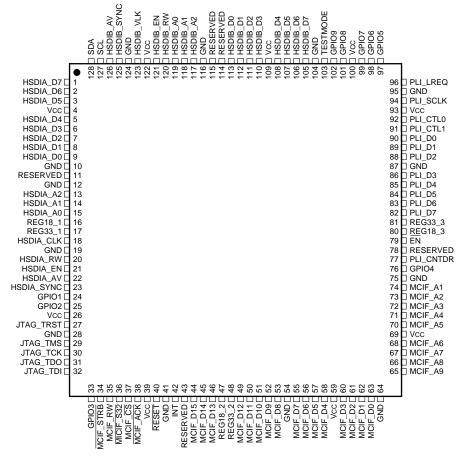
• Pin Function

No.	Pin Name	I/O	Pin Function		Pin Name	I/O	Pin Function
1	TEST11			37	VDD_02	_	[PAD] VDD
2	TEST12	I/O	Reserved for Test	38	SHCLK	ı	(SH) MPU clock
3	TEST13		39 VDD		VDD_01	-	[CORE] VDD
4	UPISEL0		I ² C slave address select	40	SHDATA0		(SH) data 0 (LSB)
5	UPISEL1	I	I ² C/SH interface select, L: I ² C, H: SH3	41	SHDATA1	1/0	(SH) data 1
6	TM4	I	Test configuration, connect to GND.	42	SHDATA2	1/0	(SH) data 2
7	MVSW	I	Reserved for Test	43	SHDATA3		(SH) data 3
8	VDD_00	_	[CORE] VDD	44	VDD_03	-	[PAD] VDD
9	SRN	I	System reset	45	GND_04	-	[PAD] GND
10	SCL	I	I ² C bus clock	46	SHDATA4		(SH) data 4
11	SDA	I/O	I ² C bus serial data	47	SHDATA5	1/0	(SH) data 5
12	NOSTDV	0	Non-standard & no-signal detect output	48	SHDATA6	1/0	(SH) data 6
13	CPULSE	0	Clamp pulse output	49	SHDATA7		(SH) data 7 (MSB)
14	HSYOUT	0	H sync output	50	GND_05	-	[CORE] GND
15	VSYIN	I	V sync input	51	PDA0		Pixel data output A0
16	GND_01	_	[CORE] GND	52	PDA1	0	Pixel data output A1
17	CLK27I	I	External clock input (27MHz)	53	PDA2		Pixel data output A2
18	VCC_S0	_	[CORE] VCC	54	VCC_S1	-	[PAD] VCC
19	GND_S0	_	[CORE] GND	55	GND_S1	-	[PAD] GND
20	XI	I	Crystal input (27MHz)	56	PDA3		Pixel data output A3
21	XO	0	Crystal output (27MHz)	57	PDA4	0	Pixel data output A4
22	GND_03	_	[CORE] GND	58	PDA5		Pixel data output A5
23	SHCS1	ı	(SH) chip select 1	59	PDA6		Pixel data output A6
24	SHCS2	'	(SH) chip select 2	60	VDD_04	-	[CORE] VDD
25	SHRD	I	(SH) read strobe	61	PDA7		Pixel data output A7
26	SHWAIT	I	(SH) wait	62	PDA8	0	Pixel data output A8
27	SHWR	I	(SH) write strobe	63	PDA9		Pixel data output A9
28	GND_02	I	[PAD] GND	64	GND_06	-	[PAD] GND
29	SHADR00		(SH) address 0 (LSB)	65	CLK270	0	27MHz clock output
30	SHADR01		(SH) address 1	66	VDD_05	_	[PAD] VDD
31	SHADR02		(SH) address 2	67	PDB0		Pixel data output B0
32	SHADR03	1	(SH) address 3	68	PDB1	0	Pixel data output B1
33	SHADR04	!	(SH) address 4	69	PDB2		Pixel data output B2
34	SHADR05		(SH) address 5	70	PDB3		Pixel data output B3
35	SHADR06		(SH) address 6	71	GND_07	-	[PAD] GND
36	SHADR07		(SH) address 7 (MSB)	72	PDB4	0	Pixel data output B4

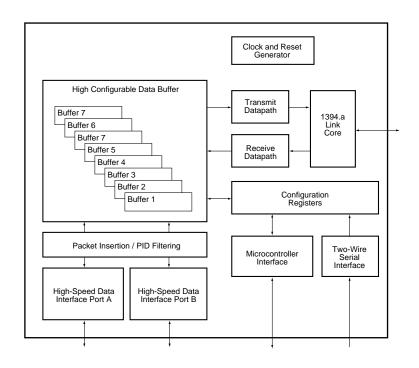
No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function	
73	PDB5		Pixel data output B5	109	TEST07	1/0	Dance and for Took	
74	PDB6	0	Pixel data output B6	110	TEST08	1/0	Reserved for Test	
75	PDB7		Pixel data output B7	111	SCAN_W		For each test, connect to VDD	
76	VDD_06	_	[CORE] VDD	112	SCAN_T	1 '	For scan test, connect to VDD.	
77	GND_08	-	[CORE] GND	113	CLKSEL	ı	Clock select L: XI, H: CLK27I	
78	PDB8	0	Pixel data output B8	114	TM1	ı	Test configuration, connect to GND.	
79	PDB9		Pixel data output B9	115	GNDA_0	-	Analog GND	
80	PT0		Pixel timing signal output 0	116	VCLMPC	-	C/CbCr clamp reference voltage input	
81	PT1	I/O	Pixel timing signal output 1	117	VDDA_0	-	Analog VDDA	
82	PT2		Pixel timing signal output 2	118	CBIN	I	Cb signal input	
83	VDD_07	-	[PAD] VDD	119	GNDA_1	-	Analog GND	
84	GND_09	-	[PAD] GND	120	CRIN	ı	Cr signal input	
85	PT3		Pixel timing signal output 3	121	VDDA_1	_	Analog VDDA	
86	PT4		Pixel timing signal output 4	122	CIN	ı	Chrominance (C) signal input	
87	PT5	I/O	Pixel timing signal output 5	123	GNDA_2	_	Analog GND	
88	PT6		Pixel timing signal output 6	124	VRTOC	-	Decupling capacitor connect pin for VRTOC	
89	PT7		Pixel timing signal output 7	125	VRBOC	-	Decupling capacitor connect pin for VRBOC	
90	VCC_S2	_	[CORE] VCC	126	VDDA_2	-	Analog VDDA	
91	GND_S2	_	[CORE] GND	127	BIAS	_	Resistor connect pin for ADC bias current	
92	PT8	1/0	Pixel timing signal output 8	128	VRB	ı	Bottom reference voltage input for ADC	
93	PT9	I/O	Pixel timing signal output 9	129	VR1	-	Decupling capacitor connect pin for VR1	
94	ACV	0	PWM output for Y clamping reference voltage	130	VRT	ı	Top reference voltage input for ADC	
95	AGCP	0	PWM output for external VCA control (positive)	131	VDDA_3	-	Analog VDDA	
96	AGCN	0	PWM output for external VCA control (negative)	132	GNDA_3	_	Analog GND	
97	GSEL	0	GSEL control signal output	133	VRBOY	_	Decupling capacitor connect pin for VRBOY	
98	VDD_08	-	[PAD] VDD	134	VRTOY	_	Decupling capacitor connect pin for VRTOY	
99	GND_10	_	[PAD] GND	135	CVBSIN	I	CVBS/Y signal input	
100	TEST00			136	VDDA_4	_	Analog VDDA	
101	TEST01			137	VCLMPY	I	CVBS/Y clamp reference voltage input	
102	TEST02				138	GNDA_4	-	Analog GND
103	TEST03	1/0	Reserved for Test	st 139 TM2		Test configuration, connect to GND.		
104	TEST04			140	140	TM3] '	rest configuration, confiect to GND.
105	TEST05				TEST09	1/0	Decembed for Took	
106	TEST06			142	TEST10	1 "/0	Reserved for Test	
107	VDD_09	-	[PAD] VDD	143	VDD_10	-	[PAD] VDD	
108	GND_11	-	[PAD] GND	144	GND_00	-	[PAD] GND	

■ TSB42AB4PDT (MAIN ASSY : IC9001)

- IEEE1394 Link IC
- Pin Assignment (Top view)



Block Diagram



• Pin Function (1/3)

No.	Pin Name	I/O	Pin Function
1	HSDIA_D7		(MSB)
2	HSDIA_D6	1/0	LICDI part A data hua
3	HSDIA_D5		HSDI port A data bus
4	Vcc	_	3.3V power supply
5	HSDIA_D4		
6	HSDIA_D3		
7	HSDIA_D2	1/0	HSDI port A data bus
8	HSDIA_D1		
9	HSDIA_D0		(LSB)
10	GND	-	Ground
11	RESERVED	_	Reserved for future use Leave unconnected.
12	GPIO0	I/O	General-purpose I/O
13	HSDIA_A2		(MSB)
14	HSDIA_A1	ı	HSDI port A address bus
15	HSDIA_A0		(LSB)
16	REG18_1	0	Internal 1.8V regulator output
17	REG33_1	1	Internal voltage regulator input
18	HSDIA_CLK	I	HSDI port A clock (Data is clocked on the rising clock edge.)
19	GND	_	Ground
20	HSDIA_R/XW	ı	HSDI port A read/write signal Used to indicate either a host read or a host write transaction to the HSDIA port.
21	HSDIA_EN	ı	HSDIA port access enable Used to indicate valid data for 1394 transmit (host writer) or 1394 receive (host read) operations.
22	HSDIA_AV	0	HSDI port A data available Used during 1394 receive operations.
23	HSDIA_SYNC	I/O	HSDI port A synchronization signal Used to determine data packet boundaries.
24	GPIO1	1/0	General-purpose I/O
25	GPIO2		General-pulpose I/O
26	Vcc	-	3.3V power supply
27	JTAG_TRST	I	JTAG test reset
28	GND	_	Ground
29	JTAG_TMS	I	JTAG test mode select
30	JTAG_TCK	I	JTAG clock
31	JTAG_TDO	0	JTAG data output
32	JTAG_TDI	I	JTAG data input
33	GPIO3	I/O	General-purpose I/O
	XMCIF_STRB	I	Data strobe signal
	MCIF_RW	I	Read/write indicator Indicates whether the current pending access is a read or a write.
	XMCIF_S32	I	Data transfer size indicator Indicates whether the host controller desires 16-bit or 32-bit transactions.
37	XMCIF_CS	I	CeLynx chip select
38	XMCIF_ACK	0	Acknowledge signal Indicates to the host controller the completion of the current read or write access.
39	Vcc		3.3V power supply
40	XRESET	I	Reset input This signal is active low.
41	GND		Ground
42	XINT	0	Interrupt This is the ceLynx interrupt output to the host.

• Pin Function (2/3)

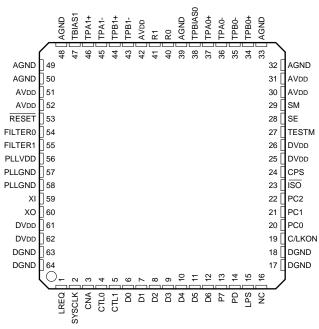
No.	Pin Name	I/O	Pin Function					
43	RESERVED	-	Reserved for future use Leave unconnected.					
44	MCIF_D15		(MSB)					
45	MCIF_D14	1/0	ficrocontroller interface bidirectional data bus					
46	MCIF_D13		interest interface pidirectional data pas					
47	REG18_2	0	Internal 1.8V regulator output					
48	REG33_2	ı	Internal voltage regulator input					
49	MCIF_D12							
50	MCIF_D11	1						
51	MCIF_D10	1/0	Microcontroller interface bidirectional data bus					
52	MCIF_D9	1						
53	MCIF_D8	1						
54	GND	-	Ground					
55	MCIF_D7							
56	MCIF_D6	1,,	Manage desilies interfered biding of a selection of the second					
57	MCIF_D5	 I/O	Microcontroller interface bidirectional data bus					
58	MCIF_D4							
59	Vcc	-	3.3V power supply					
60	MCIF_D3							
61	MCIF_D2	1.,	Migrocontroller interface hidirectional data hus					
62	MCIF_D1	 I/O	Microcontroller interface bidirectional data bus					
63	MCIF_D0	1	(LSB)					
64	GND	-	Ground					
65	MCIF_A9		(MSB)					
66	MCIF_A8	1.						
67	MCIF_A7	 	Microcontroller interface address bus					
68	MCIF_A6	1						
69	Vcc	-	3.3V power supply					
70	NCIF_A5							
71	MCIF_A4	1						
72	MCIF_A3	1	Microcontroller interface address bus					
73	MCIF_A2							
74	MCIF_A1	1	(LSB)					
75	GND	_	Ground					
76	GPIO4	I/O	General-purpose I/O					
77	PLI_CNTDR	I/O	Contender signal					
78	RESERVED	-	Reserved for future use Leave unconnected.					
79	XEN	ı	Internal power supply enable Active low.					
80	REG18_3	0	Internal 1.8V regulator output					
81	REG33_3	ı	Internal voltage regulator input					
82	PLI_D7		(LSB)					
83	PLI_D6	1/0	PHY-link data bus					
84	PLI_D5	1	and said said					

• Pin Function (3/3)

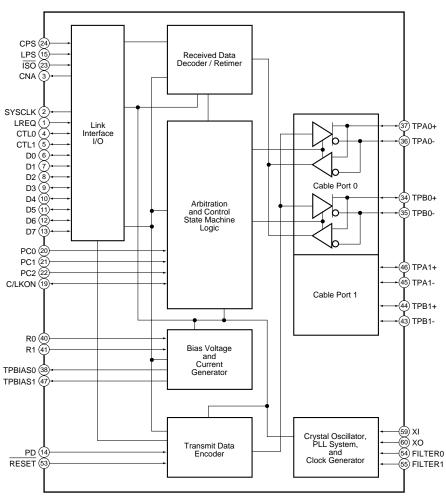
No.	Pin Name	1/0	Pin Function							
	PLI_D4		T III I WINGION							
	PLI_D3	I/O	PHY-link data bus							
87	GND	_	Ground							
	PLI_D2									
	PLI_D1	I/O	PHY-link data bus							
	PLI_D0	., 0	(MSB)							
	PLI_CTL1		(LSB)							
92	PLI_CTL0	I/O	PHY-link interface control signals (MSB)							
93	Vcc		.3V power supply							
			Physical layer system clock Supplied by the physical layer device and is 49.125MHz.							
94	PLI_SCLK	ı	PLI_SCLK is required for link layer operation.							
95	GND	-	Ground							
96	PLI_LREQ	0	Link request Requests the physical layer controller to perform some service.							
97	GPIO5									
98	GPIO6	I/O	General-purpose I/O							
99	GPI07									
100	Vcc	_	3.3V power supply							
101	GPIO8	2	Constal surpose I/O							
102	GPIO9	I/O	General-purpose I/O							
103	TESTMODE	I	Factory test pin Connect to GND for normal device operation.							
104	GND		Ground							
105	HSDIB_D7		(MSB)							
106	HSDIB_D6									
107	HSDIB_D5	I/O	HSDI port B data bus							
	HSDIB_D4									
109	Vcc	_	3.3V power supply							
110	HSDIB_D3									
	HSDIB_D2	I/O	HSDI port B data bus							
112	HSDIB_D1									
113	HSDIB_D0		(LSB)							
114	RESERVED		Reserved for future use Leave unconnected.							
115	RESERVED	_	Reserved for future use Leave unconnected.							
116	GND	_	Ground							
117	HSDIB_A2		(MSB)							
118	HSDIB_A1	ı	HSDI port B address bus							
119	HSDIB_A0		(LSB)							
	HSDIB_R/XW	ı	HSDI port B read/write signal Used to indicate either a host read or a host write transaction to the HSDIB port.							
121	HSDIB_EN	ı	HSDIB port access enable Used to indicate valid data for 1394 transmit (host writer) or 1394 receive (host read) operations.							
122	Vcc	1	3.3V power supply							
123	HSDIB_CLK	I	HSDI port B clock (Data is clocked on the rising clock edge.)							
124	GND	_	Ground							
125	HSDIB_SYNC	I/O	HSDI port B synchronization signal Used to determine data packet boundaries.							
126	HSDIB_AV	0	HSDI port B data available Used during 1394 receive operations.							
127	SDA	ı	Serial interface data input signal Used during ceLynx power up and reset to auto configure CFRs.							
128	SCL	0	Serial interface clock							
	l									

■ TSB41AB2PAP (MAIN ASSY : IC9002)

- IEEE1394 Physical IC
- Pin Assignment (Top view)



Block Diagram



• Pin Function

No.	Pin Name	I/O	Pin Function		Pin Name	1/0	Pin Function	
1	LREQ	I	LLC request input The LLC uses this input to initiate a service request to the TSB41AB2.		AGND	_	Analog ground	
2	SYSCLK	0	System clock output (49.152MHz)		TPB0-			
3	CNA	0	Cable-not-active input This pin is asserted high when there are no ports receiving incoming bias voltage.	35	TPB0+	I/O	Twisted-pair cable B differential signal	
4	CTL0	I/O	Control I/Os These bidirectional signals control communication between the TSB41AB2 and the LLC.		TPA0-	1/0	Twisted-pair cable A differential signal	
5	CTL1	1/0			TPA0+	1/0	Twisted-pair cable A differential signal	
6	D0			38	TPBIAS0	I/O	Twisted-pair bias output	
7	D1		Data I/Os		AGND	-	Analog ground	
8	D2				R0		For current setting resistor	
9	D3	1/0			R1	-		
10	D4	I/O	These are bidirectional data signals between the TSB41AB2 and the LLC.	42	AVDD	-	Analog power supply	
11	D5			43	TPB1-	1/0	Twisted pair cable D differential signal	
12	D6				TPB1+	1/0	Twisted-pair cable B differential signal	
13	D7				TPA1-	1/0	Twisted pair cable A differential size -	
14	PD	ı	Power down input	46	TPA1+	1/0	Twisted-pair cable A differential signal	
15	LPS	ı	Link power status input	47	TPBIAS1	I/O	Twisted-pair bias output	
16	NC	_	Not used	48	AGND			
17	DGND		Digital ground		AGND	_	Analog ground	
18	DGND	_			AGND			
19	C/LKON	I/O	Bus manager contender programming input and link-on output	51	AVdd	_	Analog power supply	
20	PC0		Power class programming inputs		AVdd			
21	PC1	I			XRESET	ı	Logic reset input	
22	PC2				FILTER0	1/0	PLL filter	
23	XISO	ı	Link interface isolation control input	55	FILTER1	1,0	i LE intoi	
24	CPS	I	Cable power status input This circuit drives an internal comparator that is used to detect the presence of cable power.	56	PLLVDD	_	PLL circuit power supply	
25	DVdd			57	PLLGND		DIL sinovit susuad	
26	DVdd	_	Digital power supply		PLLGND	-	PLL circuit ground	
27	TESTM		Test control input		ΧI		Crystal oscillator inputs	
28	SE	ı			хо	-		
29	SM				DVDD		Digital power august	
30	AVdd				DVDD	-	Digital power supply	
31	AVdd	_	Analog power supply	63	DGND		District account	
32	AGND	-	Analog ground	64	DGND	-	Digital ground	

■ PE7003B (MAIN ASSY : IC9501)

• DMA I/F LSI

• Pin Function (1/2)

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function		
1	SCANEN	I	For ATPG (Pull-down normally)	43	TESTFNC8				
2	ATPQEN	I	For ATPG (Pull-down normally)	44	TESTFNC9				
3	Vss	_	GND	45	REQDI	0	Input REQ		
4	VDD	_	3.3V power supply	46	Vss	-	GND		
5	RESET	ı	Reset	47	VDD	-	3.3V power supply		
6	TEST_MON0	0	Test monitor output 0	48	ACKDI	ı	Input ACK		
7	TEST_MON1	0	Test monitor output 1	49	DATADI0	ı	Input data 0		
8	NEW_CLKIN	ı	Input/output CLK	50	DATADI1	ı	Input data 1		
9	NEW_GND	_	GND	51	DATADI2	I	Input data 2		
10	TEST_MON2	0	Test monitor output 2	52	DATADI3	I	Input data 3		
11	TEST_MON3	0	Test monitor output 3	53	DATADI4	I	Input data 4		
12	REQEI_0	0	Don't use	54	DATADI5	I	Input data 5		
13	ACKEI_1	0	Input REQ	55	DATADI6	I	Input data 6		
14	Vss	_	GND	56	DATADI7	I	Input data 7		
15	VDD	_	3.3V power supply	57	Vss	-	GND		
16	TEST_MON4	0	Test monitor output 4	58	VDD	-	3.3V power supply		
17	REQEI_1	I	Input REQ	59	TESTFNC10				
18	RWEI	I	Don't use (Pull-up)	60	TESTFNC11				
19	DATAEI_0	ı	Input data 0	61	TESTFNC12				
20	DATAEI_1	ı	Input data 1	62	TESTIN0	ı	Test input 0		
21	DATAEI_2	ı	Input data 2	63	TESTIN1	I	Test input 1		
22	DATAEI_3	ı	Input data 3	64	IRQ	0	IRQ (Interrupt Request) signal output		
23	DATAEI_4	I	Input data 4	65	D0	I/O	Data bus 0		
24	DATAEI_5	I	Input data 5	66	D1	I/O	Data bus 1		
25	DATAEI_6	I	Input data 6	67	Vss	-	GND		
26	DATAEI_7	I	Input data 7	68	VDD	-	3.3V power supply		
27	Vss	_	GND	69	D2	I/O	Data bus 2		
28	VDD	_	3.3V power supply	70	D3	I/O	Data bus 3		
29	CLK_EO	I	Input/output CLK	71	D4	I/O	Data bus 4		
30	PIN30	ı	Not used	72	D5	I/O	Data bus 5		
31	PIN31	I	Not used	73	D6	I/O	Data bus 6		
32	TESTRAM	I	For RAM test	74	D7	I/O	Data bus 7		
33	TESTNC0	I		75	Vss	_	GND		
34	TESTNC1	I		76	REQEO_0	ı	Don't use (Pull-up)		
35	Vss	_	GND	77	REQEO_1	ı	Output ACK		
36	VDD	_	3.3V power supply	78	Vss	-	GND		
37	TEST_MO	I	Test mode switch 0	79	VDD	-	3.3V power supply		
38	TESTMI	I	Test mode switch 1	80	ACKEO_0	0	Don't use (Pull-up)		
39	TESTFNC4			81	ACKEO_1	0	Output REQ		
40	TESTFNC5				RWEO	0	Don't use (Pull-up)		
41	TESTFNC6				DATAEO0	0	Output data 0		
42	TESTFNC7			84	DATAEO1	0	Output data 1		

• Pin Function (2/2)

No.	Pin Name	I/O	Pin Function
85	DATAEO2	0	Output data 2
86	DATAEO3	0	Output data 3
87	DATAEO4	0	Output data 4
88	DATAEO5	0	Output data 5
89	DATAEO6	0	Output data 6
90	DATAEO7	0	Output data 7
91	Vss	_	GND
92	VDD	-	3.3V power supply
93	A0	ı	Address bus 0
94	A1	I	Address bus 1
95	A2	ı	Address bus 2
96	A3	ı	Address bus 3
97	A4	ı	Address bus 4
98	A5	I	Address bus 5
99	Vss	_	GND
100	VDD	_	3.3V power supply
101	A6	I	Address bus 6
102	A7	I	Address bus 7
103	RD	ı	RD (CPU)
104	WR	ı	WR (CPU)
105	cs	ı	CS (CPU)
106	CLK	ı	Master CLK
107	Vss	_	GND
108	REQDO1	I	Output REQ
109	REQDO2	I	Don't use (Pull-down)
110	Vss	_	GND
111	VDD	-	3.3V power supply
112	ACKDO	0	Output ACK
113	DATADO0	0	Output data 0
114	DATADO1	0	Output data 1
115	DATADO2	0	Output data 2
116	DATADO3	0	Output data 3
117	DATADO4	0	Output data 4
118	DATADO5	0	Output data 5
119	DATADO6	0	Output data 6
120	DATADO7	0	Output data 7
121	Vss	_	GND
122	VDD	-	3.3V power supply
123	TSTEN	_	Not used
124	TCK	ı	Not used (Pull-up)
125	TDI	ı	Not used (Pull-up)
126	TMS	I	Not used (Pull-up)
127	TDO	0	Not used (Connection prohibition)
128	TRST	I	Not used (Pull-up)

■ PDY078A (MAIN ASSY : IC9503)

• CMOS EPLD

• Pin Function (1/2)

No.	Pin Name	I/O	Pin Function	Connection Point	No.	Pin Name	I/O	Pin Function	Connection Point
1	OUREMP	ı	FIFO empty flag	PE7003B	33	GND	_	GND	
2	EBSACK_X	I	DMA acknowledge	PE7003B	34	VCCIO	-	VCC	
3	VCCIO	-	VCC		35	I_DATA6	0	Record system stream	IC9502
4	TDI				36	I_DATA7			109502
5	EBSDW0		I Record system stream		37	IRDY1_X	ı	Input ready	IC9502
6	EBSDW1				38	GND	_	GND	
7	EBSDW2			DVxcel	39	VCCINT			
8	EBSDW3	'		Dyxcei	40	OEN1_X	ı	Output enable	IC9502
9	EBSDW4				41	ORDY1	0	Output ready	IC9502
10	EBSDW5				42	RD_DAT_X0	0	Record system stream	IC9502
11	GND	-	GND		43	GND	-	GND	
12	EBSDW6	ı	Record system stream	DVxcel	44	RD_DAT_X1		Record system stream	IC9502
13	EBSDW7	'	Record system stream		45	RD_DAT_X2			
14	EDMARQ	I	DMA request	DVxcel	46	RD_DAT_X3	I		
15	TMS				47	RD_DAT_X4			
16	AVDACK	I	DMA acknowledge	PE7003B	48	RD_DAT_X5			
17	OUMAAND	I	DMA request	PE7003B	49 RD_DAT_X6				
18	VCCIO	-	VCC		50	RD_DAT_X7			
19	OUDREQ				51	VCCIO	ı	vcc	
20	AVDREQ	I	DMA request	M65774AFP	52	IEN1	0	Input enable	IC9502
21	AVDREQX	0	DMA request	PE7003B	53	GND	ı	GND	
22	WAITDVX	I	CPU wait	DVxcel	54	OUWMD_X0		Record system stream	PE7003C
23	WAITDVSH	0	DVxcel wait NG	SH3	55	OUWMD_X1			
24	LIOR0	0	Read	IC9502	56	OUWMD_X2	ı		
25	LIOW0		Write	IC9502	57	OUWMD_X3			
26	GND	_	GND		58	OUWMD_X4			
27	I_DATA0		D Record system stream IC9502		59	GND	-	GND	
28	I_DATA1	0			60	OUWMD_X5	1	Record system stream	DVxcel
29	I_DATA2			IC9502	61	OUWMD_X6			
30	I_DATA3				62	TCK			
31	I_DATA4			63	OUWMD_X7	ı	Record system stream	DVxcel	
32	I_DATA5				64	WMOUACK	ı	DMA acknowledge	PE7003B

• Pin Function (2/2)

No.	Pin Name	I/O	Pin Function	Connection Point
65	GND	_	GND	
66	VCCIO	_	VCC	
67	WMOURQ_X	I	DMA request	DVxcel
68	OUWMRQ	0	DMA request	PE7003B
69	DVFRM	I	DV frame sync	TSB42AA4PTD-5C
70	DVOEN	I	Output enable	SH3
71	XCS42	ı	Chip select	PE5219A
72	LRDWR	ı	Read/write	SH3
73	TDO			
74	GND	-	GND	
75	MKBRD	ı	DMA flag	SH3
76	WAITWM	ı	CPU wait	High level fixing
77	GPIO3_WM0	ı	FIFO full flag	TSB42AA4PTD-5C
78	GND	_	GND	
79	TBCLK	0	6.75MHz clock	DVxcel
80	HSDIA_CLK	0	6.75MHz clock	TSB42AA4PTD-5C
81	27MSEL	ı	27MHz clock	
82	VCCIO	_	vcc	
83	DVCSEL	ı	DV I/O switch	PE5108A
84	MCIF_STRBZ	0	Strobe	TSB42AA4PTD-5C
85	MCIF_ACKZ	ı	Acknowledge	TSB42AA4PTD-5C
86	GND	_	GND	
87	40MPLD	ı	40MHz clock	
88	XRESET	ı	Reset	
89	LXWE0	ı	Write enable	SH3
90	LXRD	_	Read	SH3
91	VCCIO	_	vcc	
92	SELVR	ı	VR-VIDEO select	SH3
93	LXCS56	ı	Chip select	PE5219
94	HSDIA_EN	0	Request	TSB42AA4PTD-5C
95	GND	_	GND	
96	HSDIA_AV	ı	Acknowledge	TSB42AA4PTD-5C
97	XWAITDV	0	CPU wait	PE5219A
98	DVACK	0	Acknowledge	DVxcel
99	DVREQ	I	Request	DVxcel
100	XWAITBY	Ι	CPU wait	PE5108A

■ UPD65944GC-E59-7EA (MAIN ASSY : IC9502)

• Stream Check IC

• Pin Function

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	26	GND	51	VDD	76	GND
2	CLK	27	TP03	52	PO_EN1	77	TP11
3	GND	28	TP02	53	PO_RDY1	78	I_DAT7
4	LCS0	29	TP01	54	TP_SEL0	79	I_DAT6
5	TP06	30	TP00	55	RO_EN1	80	I_DAT5
6	LIOW0	31	SCK	56	RO_RDY1	81	I_DAT4
7	TP16	32	AMC	57	RO_DAT7	82	TP10
8	TP05	33	TP14	58	INT	83	I_DAT3
9	LIOR0	34	TP13	59	RO_DAT6	84	I_DAT2
10	LWAIT0	35	PO_DAT7	60	GND	85	I_DAT1
11	LDB7	36	TP12	61	RO_DAT5	86	I_DAT0
12	LDB6	37	PO_DAT6	62	RO_DAT4	87	TP09
13	TEB0	38	GND	63	VDD	88	VDD
14	LDB5	39	PO_DAT5	64	RO_DAT3	89	TP18
15	GND	40	TP_SEL4	65	RO_DAT2	90	TP17
16	LDB4	41	PO_DAT4	66	GND	91	LAB06
17	SMC	42	TP_SEL3	67	RO_DAT1	92	TP08
18	TIN	43	PO_DAT3	68	RO_DAT0	93	LAB05
19	TP04	44	TP_SEL2	69	SIMMOD0	94	LAB04
20	LDB3	45	PO_DAT2	70	I_EN1	95	LAB03
21	LDB2	46	VDD	71	I_RDY1	96	TP07
22	TP15	47	PO_DAT1	72	RST0	97	LAB02
23	LDB1	48	TP_SEL1	73	GND	98	LAB01
24	LDB0	49	PO_DAT0	74	EX_CLK	99	LAB00
25	VSS	50	GND	75	VDD	100	GND

7.3 OUTLINE OF THE PRODUCT

7.3.1 DVD-RW Standard

The DVD-RW disc is a phase-change type, rewritable disc, as are CD-RW and DVD-RAM discs. In playback of a phase-change type disc, signals that are obtained through the change in reflectivity between crystalline and amorphous states of the recording layer can be read by the optical system employed in playback-only players. Fig. 1 shows the structure of a DVD-RW disc. On a 0.6-mm-thick polycarbonate molded substrate, an Ag-In-Sb-Te-alloy recording layer, a protective layer, and a reflective layer are deposited.

DVD-RW uses CLV-type groove-recording format, and employs the wobble groove & land pre-pit system, as does DVD-R, for rotation control and address information during recording.

For this, so-called LPPs (Land Pre-Pits) are provided on certain locations in the land areas, and the groove has a minutely undulating structure called "wobble." The wobble is mainly used for rotation control of the disc, and the frequency of the wobble signal is 8 times that of the sync frame (8 cycles in one sync frame). LPPs are located from the first to the third bits of the sync frame at the maximum oscillation of the wobble, and these three bits and one ECC (error correction code) comprise preaddress information.

Table 1 shows the basic specifications of DVD-RW. The specifications, such as the form of the disc, 4.7 GB/side recording capacity, 0.4 μ m minimum pit length, 0.74 μ m track pitch, modulation method, and error-correcting code, are the same as those of DVD-ROM. The recording and playback wavelengths are both 635/650 nm.

As to the characteristics after recording, the reflectivity is within the standard value of a dual-type DVD-ROM, and the specifications for modulation and jitter are the same as those of DVD-ROM format. Moreover, as the tracking system during playback, phase-difference tracking is employed, analogous to DVD-ROM.

Table 1 Basic Specifications of DVD-RW

Specifications of DVD-RW	Specifications of DVD-ROM
Phase Change	Read Only
Re-writable	-
120/80mm	←
Wobble & LPP	
CLV	←
4.7G/1.46Gbytes	
	8.54Gbytes **
11.08Mbps	\leftarrow
635/650nm	
635/650nm	←
– 15 mW	
0.74 μm	←
0.4 μm	←
8-16 Modulation	←
18 – 30%	45-85%*
	18-30%**
Option	
	of DVD-RW Phase Change Re -writable 120/80mm Wobble & LPP CLV 4.7G/1.46Gbytes 11.08M bps 635/650nm 635/650nm - 15 mW 0.74 µm 0.4 µm 8-16 Modulation 18 - 30 %

^{*} Single Layer Disc

^{**} Dual Layer Disc

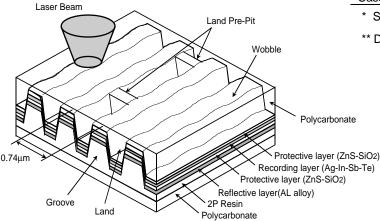


Fig. 1 Structure of DVD-RW disc

7.3.2 Video Recording Format

The DVD Forum created the DVD-Video format as an application format. As this format was created mainly for the authoring systems for a PC environment and intended to reduce the burden on playback-only players, its data structure is not suitable for real-time recording. As the DVD-Video format was for ROM discs, which do not require addition of descriptions or edition by users, its fairly complex structure posed little trouble for authoring systems. Therefore, the format contained various items that allowed content producers to use various functions, such as multiangle, multistory, various menus, multilanguage, commands, and high picture/sound quality.

In comparison, in considering the use for general users' recording/playback use, such as VCR, Camcorder, and MD, the Video Recording format was defined to respond to the following requests:

- 1. Real-time recording
- 2. Easy to edit/operate
- 3. High picture quality
- 4. Efficient usage of available area on a disc

Table 2 shows the outline of Video Recording format data.

Table 2 General Specifications of Presentation Data

Data Systems	MPEG-2 system stream / program stream Maximum program_mux_rate = 10.08Mbps						
Video	number of stream compression bit rate MPEG-2 MPEG-1		: 1 : Complies with MPEG-2 or MPEG-1 : 9.80 Mbps or less : 1.856 Mbps or less				
Audio	number of streams coding mode	: 2 max : Linear PCM / Dolby AC-3 / MPEG					
	Linear PC		Dolby AC-3 MPEG-1		MPEG-2		
	sampling frequency	48kHz	48kHz	48kHz	48kHz		
	bits per sample	16bits	compressed	compressed	compressed		
	bit rate (max.)	1.536Mbps	448 kbps 384kbps		912kbps		
	number of channels	2 max.	5.1 max.	2 max.	7.1 max.		
Sub-picture	number of streams data type data size of a picture display area TV system with 525 / 60 TV system with 625 / 50	: 52KB max. : a rectangula	coded bitmap , 2-bit/pixel ar in a frame : 720(H) × 478(V) max. : 720(H) × 537(V) max.				
	colors : 16 colors pa				6 colors palette for each VOB		

Fig. 2 shows a recorded content model. The original represents an image of a group of titles previously recorded on a VCR and now actually recorded on a disc. Up to 99 titles can be recorded on a disc. A title may be actually recorded on noncontinuous areas, but for users, it appears to be recorded continuously.

The play list is a program created from time information of actual original titles, and a virtual title is composed only of management information.

Any portions of titles can be selected in any order with accuracy to one video frame in a play list. Up to 99 play lists can be created. Both original titles and play lists can contain chapters.

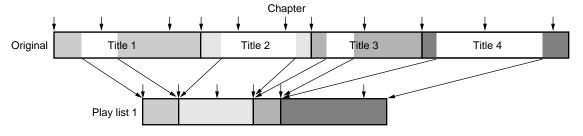


Fig. 2 Recorded content model

7.3.3 Main Newly Developed Features 7.3.3.1 Pickup

In addition to DVD-R/RW recording and DVD-ROM playback, the newly developed pickup can play back CD media. The laser diodes are provided separately for DVD and CD, but one lens is used for both.



Fig. 3 Pickup

7.3.3.2 LSI for Process of Recording Signals

The conventional structure of 3 chips and a discrete circuit has been integrated into 2 chips, realizing performance stabilization and cost reduction.



RECORDER DRIVE MAIN IC109 PM0025AF



RECORDER DRIVE MAIN IC602 PE5131A

Fig. 4 A2-Chip R3-Chip

7.3.3.3 Video Decoder LSI

A video decoder LSI for high-quality conversion of analog video signals to digital signals has been newly developed. By mounting a 10-bit/27-MHz video ADC, higher accuracy and better stabilized reproduction of luminance and color have been realized.



MAIN Assy IC8008 PD0272A

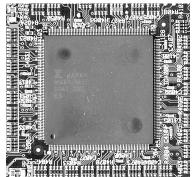
Fig. 5 George

7.3.3.4 MPEG Video Encoder LSI

A new MPEG video encoder LSI, which enables recording in 3/4-D1 and 2/3-D1 resolutions in addition to conventional full-D1 and 1/2-D1 resolutions available with the conventional MPEG-2 encoders, has been developed. This offers more options of resolutions suited to length of recording, and enables higher picture quality even with longer recording. It also reduces load on the host CPU by substituting multiplexed processing of video and audio data for it, and contributes to cost reduction by assuming the DV codec function.

7.3.3.5 Graphics Engine LSI

An LSI for graphics processing, such as full-resolution GUI and the reduced-size-moving-picture-capture function, has been newly developed for easier operation and an easy-to-understand user interface. This can dramatically improve UI expression. This LSI also has high-quality picture features, such as frame TBC (Time Base Corrector) and 3DNR (Digital Noise Reduction).



MAIN Assy IC4006 PD6342A

Fig. 4 Vaikilt

7.3.3.6 Drive Interface LSI

Conventionally, SCSI was employed as a drive interface, and was controlled by a dedicated LSI and CPU. Transfer of data was managed by the host CPU.

Now, ATAPI has been employed as the drive interface, and a new LSI has been developed. By transferring management of data transfer to the LSI, drive-control functions have been converged to the LSI, thus reducing load on the host CPU and contributing to cost reduction.



MAIN Assy IC3003 PE5219A

Fig. 7 Slalom

7.3.3.7 LPCM Audio Recording

The DDCE (Dolby Digital Consumer Encoder) has been conventionally employed for audio encoding, and now LPCM (Linear PCM) audio recording has been created as an algorithm for AV encoding, enabling audio recording more faithful to the original sound

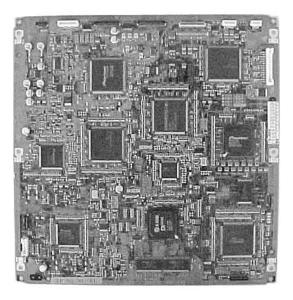


Fig. 8 MAIN Assy

7.3.4 System Control Structure

Fig. 9 shows a system block diagram of the DVR-7000. The system is roughly divided into two blocks: the writer block (which writes in and reads out data to and from a disc), and the recorder block (which encodes/decodes video and audio signals and generally controls the whole system, including UI).

7.3.4.1 Structure of the Control System

Although the DVR-2000 contained 6 CPUs, including the one controlling DV, the DVR-7000 contains the following 3 CPUs (see Fig. 10):

- Recorder Main CPU
 For control of the whole system, such as recording and playback operations, including control of each CPU, and user interface
- Read/Write Control CPU
 For control of read out/write in from/to a disc.
- (3) Tuner/FL Control CPU
 For control of the tuner, FL, 3-D Y/C, and keys of the main unit, and for management of time and timer setting

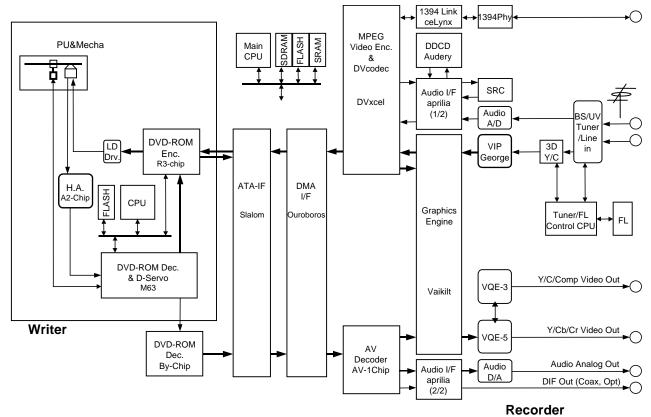


Fig. 9 System block diagram

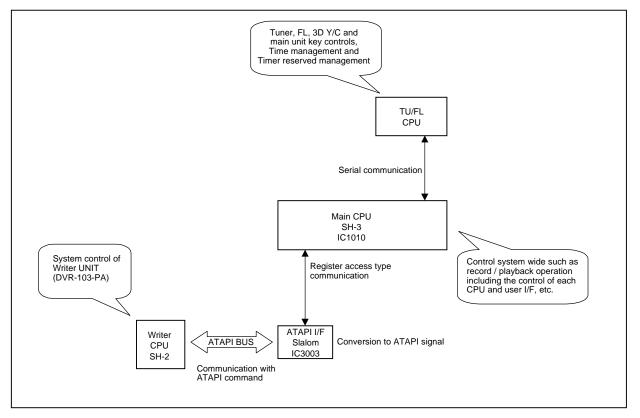


Fig. 10 CPU control share

7.3.4.2 Recording System

The basic flow of data with the DVR-7000 is similar to that with the DVR-2000. Recordable media are DVD-R (Ver. 2.0) and DVD-RW (Ver. 1.0/1.1), and recording application formats are Video Recording Format (DVD-VR) and Video Mode Recording Format. Only Video Mode Recording is possible with DVD-R discs, and DVD-VR recording is possible with DVD-RW discs (Video Mode Recording is also possible with Ver. 1.1 DVD-RW discs). The available recording speed to discs is normal speed.

In DVD-VR recording, analog video and audio line input signals or analog video and audio signals detected by the tuner are ADconverted, input to the Graphics Engine LSI, processed with the frame TBC and 3DNR, then encoded and multimplexed in real time. In the video and audio encoding block, based on the set recording length or recording bit rate, the most suitable encoding parameter is determined, and MPEG video encoding is made by variable bit rate (VBR). Compressed video stream and audio stream compressed by DDCE (Dolby Digital Consumer Encoder) are then packed and multiplexed, and are formed into a basic VOB (video object) conforming to the Video Recording Format. In the video stream, necessary information stipulated in the Video Recording Format, such as RDI (Real-time Data Information) in a VOB, is described. Everything up to this process is done by the MPEG Encoder LSI. A stream sent from this MPEG Encoder LSI is temporarily stored in the SDRAM (stream buffer) of the ATAPI interface LSI. The main CPU controls transfer so that the downstream will not overflow, and the temporarily stored stream is then transferred to the writer block via the ATAPI bus. As actual recording to a disc is done intermittently, a write command is issued when data reach certain amount, and a mass of data are transferred simultaneously.

The data is formatted into the DVD physical format in the DVD-ROM encoder of the writer block, then actually recorded on a disc with the most suitable emission power of the laser diode and the strategy. On the disc, data are recorded intermittently in blocks, and these data blocks are linked with no linking loss.

In actual operation, one title is created by one sequence of a user's starting recording through stopping recording. If recording is paused, a chapter will be created. If the disc is removed from the unit, the management information (file system and VR_MANGR.IFO, etc.), which is managed by the main CPU and which is necessary to play back the recorded video and audio signals, will be recorded on the disc. Editing can be made on the originals and play lists. For editing of a play list, only management information is updated and rewritten, and VOBs are not rewritten. Thus, nondestructive editing is possible.

7.3.5 Playback System 7.3.5.1 DVD Playback

The path for transferring AV decoder data in the DVR-7000 has largely been modified from that of the DVR-2000.

The path of DVD-video playback is the same as that of conventional DVD-video playback: The RF signal read out from a disc is converted into NRZI (non return to zero inverse) signal after passing through the preamplifier, then is sent to the recorder block; There, the DVD physical format is decoded. Then in the AV decoder, the signal is decoded into digital video and audio data. This is basically the same path as that the DVD-video player uses to play back a DVD-video disc. The playback speed is normal speed.

During playback of a DVD-VR, the data-transfer path from the writer block is the same as that in recording (via the ATAPI bus).

The RF signal read out from a disc is processed up to DVD physical formatting in the writer block, transferred via the ATAPI bus, and is temporarily stored in the SDRAM (stream buffer) of the ATAPI interface LSI. Then, the data are transferred to the AV decoder and decoded to video and audio digital data. Thus, for DVD-VR, the same path is used for recording and playback during data transfer from the recorder to the writer blocks. The playback speed of DVD-VR is double normal speed (only for DVD-VR).

The AV-decoded data pass through the same path regardless of the applications used. The digital video signal enters the Graphics Engine LSI, where the overlay process with the GUI & OSD takes place. If a disc-navigation display is called by the user, video capture and multiscreen display processes are executed for the designated frame (random designation possible) of each title. Then, the digital video signal is processed with 3DNR in the NTSC Encode LSI to be output as an analog video signal.

As to the audio signal, audio digital data to be output as an analog signal are decoded in the AV decoder, and audio digital data to be output as a digital signal are DIF-modulated after being decoded in the AV decoder, then either signal goes to the AUDIO interface LSI, where the signal to be output as a digital signal undergoes a switching process, and for the signal to be output as an analog signal, data are gathered for the level meter and switching process is executed. The signal is then output through the DAC.

7.3.5.2 CD/Video-CD Playback

Playback of CD media is newly added for the DVR-7000. The basic data flow is similar to that of a DVD-video player. Playback speed of CD media is 4 times normal speed in CAV.

As to CD-DA playback, the RF signal read out from a disc is EFM-demodulated in the writer block. Then the signal to be output as an analog signal is sent to the recorder block as a 3-line serial signal of IEC60958 format, and the signal to be output as a digital signal is DIF-modulated in the writer block and then is sent to the recorder block

The signal to be output as an analog signal via the Audio interface LSI enters the SRC, where the sampling rate is converted from 44.1 kHz to 48 kHz. Then, the signal enters the Audio interface LSI again, and is finally output through the DAC. The signal to be output as a digital signal also undergoes a switching process in the Audio interface LSI, and then is output as DIF.

As to Video-CD playback, as with CD-DA playback, the RF signal read out from a disc is EFM-demodulated in the writer block. Then the CD-ROM data for Video-CD is then sent to the recorder block as a 3-line serial signal of IEC60958 format, as with the signal to be output as an analog signal. In the recorder block, the data are first decoded then sent to the AV decoder, where the data are decoded into video and audio digital data. Then, the data pass and are processed in the same way as with DVD playback and are then output.

7.3.6 Newly Added Functions and Specifications

The following functions and specifications are newly added to the DVR-7000, compared with the DVR-2000.

7.3.6.1 CD/Video-CD Playback

As mentioned before, the newly developed pickup for DVD-R/RW recording, responding to two wavelengths, makes it possible to play back CD media. The basic functions are the same as those of DVD-Video players.

7.3.6.2 Progressive Output

For the video output stage, the same chip set as that for the DV-S737 is employed, and the D2 terminal is mounted to respond to the progressive output. Therefore, the same functions as with the DV-S737, such as 2-3 pull-down progressive scan and movement-adaptable-type interpolation processing functions, are provided, and the 10-bit/54-MHz video DAC is included. It also has functions such as component-frame DNR and quantum noise reduction.

7.3.6.3 Picture Creation

The Picture Creation function, which integrally controls LSIs for video input and output and settings of various NRs and which realizes the highest recording and playback picture quality by making picture-quality settings to best suit the video content, is provided. The most suitable picture-quality setting is possible with a simple operation.

7.3.6.4 Recording in 3/4-D1 and 2/3-D1 Resolution

As mentioned before, a newly developed MPEG video encoder LSI enables recording in 3/4-D1 and 2/3-D1 resolutions in addition to the conventional full-D1 and 1/2-D1 resolutions available with the conventional MPEG-2 encoders. This offers more options of resolutions suited for length of recording, and enables higher picture quality even with longer recording.

7.3.6.5 LPCM Recording

In addition to the conventionally used DDCE, LPCM recording is provided to the DVD-recorder. This enables audio recording more faithful to the original sound. LPCM recording is possible only with MN32 recording rate.

7.3.6.6 Full-resolution GUI

The newly developed Graphics Engine LSI with full-resolution GUI functions dramatically improves the power of expression. In combination with the reduced-size-moving-picture-capture function, an easy-to-operate and high-quality User Interface has been realized.

7.3.6.7 Special Playback

To improve the operability and performance as an editing machine, various special playback functions and performance are provided. Besides frame-by-frame playback in forward and reverse, special playback functions, such as 1/2-, 1/4-, 1/8-, and 1/16-time playback in forward and reverse, and reverse playback at normal speed in full resolution are possible.

7.3.7 Other Features and Specifications

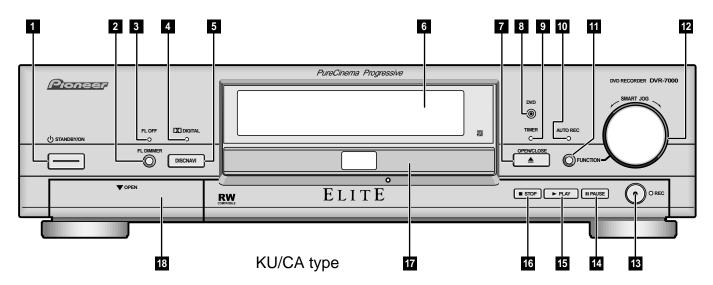
Other conventional features and specifications are as follows:

- 96-kHz/24-bit DAC
- 48-kHz/20-bit ADC
- 3-Dimensional Y/C-separation circuit
- Frame TBC
- Responding to the DV (iLink) input/output
- Built-in BS tuner
- Disc Navigator
- Disc timer
- · Commercial skip

8. PANEL FACILITIES AND SPECIFICATIONS

8.1 PANEL FACILITIES

■ FRONT PANEL



- 1 **⁶** STANDBY/ON button
- 2 FL DIMMER button Press to change the display brightness
- 3 FL OFF indicator Lights when the display is switched off using the FL DIMMER button
- 4 DOLBY DIGITAL indicator Lights when a Dolby Digital soundtrack is playing
- 5 DISCNAVI buttonPress to display the Discnavi screen
- 6 Display
- 7 OPEN/CLOSE button Press to open/close the disc tray
- 8 DVD indictor Lights when a DVD disc is loaded
- 9 TIMER indicator Lights when the record timer is set and the power is in standby
- 10 AUTO REC indicator
 Lights when the recorder has been set for automatic recording
- 11 FUNCTION button
 Press to switch the function of the SMART JOG

- 12 SMART JOG control

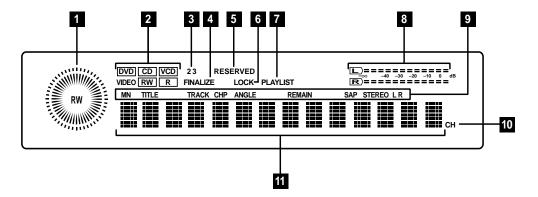
 Turn to change the parameter selected with the FUNCTION button
- 13 REC button/indicator Press to start recording
- 14 II PAUSE button

 Press to pause playback or recording
- 15 ► PLAY button Press to start or restart playback
- 16 STOP button Press to stop playback or recording
- 17 Disc tray
- 18 Front panel jacks Analog and digital input/output jacks for connecting a camcorder or other external equipment



This indicates a product feature that is capable of playing DVD-RW discs recorded with Video Recording format.

■ DISPLAY



1 Play/record indicator

Outer (white) ring indicates the playback speed and direction. Inner (red) ring indicates elapsed playback/recording time

The center RW indicator lights when a VR mode disc is loaded

2 DVD CD VCD VIDEO RW R

Shows the type of disc loaded

3 23

Shows the remote control mode (if nothing is displayed, the remote control mode is 1)

4 FINALIZE

Lights when a finalized disc is loaded

5 RESERVED

Lights when a disc containing a disc timer program is loaded

6 LOCK

Lights when the child lock is active

7 PLAYLIST

Lights when a VR mode disc is loaded and the recorder is in Playlist mode

8 Audio level indicators

Monitors the ouput audio level during playback and the input audio level during recording

9 MN

Display shows the manual rate recording level

TITLE

Display shows the current title number of the DVD disc playing

TRACK

Display shows the current track number of the CD or Video CD disc playing

CHP

Display shows the current chapter number of the DVD disc playing

ANGLE

Lights when a multiangle scene on a DVD disc is playing, indicating that you can switch angles

REMAIN

Display shows the amount of recording time available on the disc loaded

SAP

Lights when the currently selected TV channel has a Secondary Audio Program channel

STEREO

Lights when the incoming TV signal is stereo

ΙR

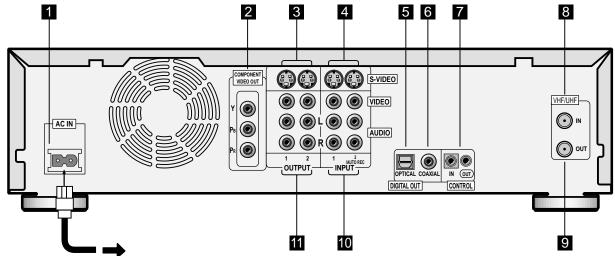
Indicates which channels are recorded/played back when Dual Mono is selected.

10 CH

Channel indicator for the built-in TV tuner

11 Character display

■ REAR PANEL



1 AC IN - Power inlet

2 COMPONENT VIDEO OUT

For connecting to a TV or monitor that has component video input

3 S-VIDEO OUTPUT 1, 2

For connecting to a TV, monitor, AV receiver or other equipment with S-Video input

4 S-VIDEO INPUT 1, 2

For recording from a camcorder, VCR or other equipment with S-Video output

5 DIGITAL OUT OPTICAL

For connecting to an AV receiver, Dolby Digital/ DTS decoder or other equipment with optical digital inpu

6 DIGITAL OUT COAXIAL

For connecting to an AV receiver, Dolby Digital/ DTS decoder or other equipment with coaxial digital input

■ FRONT TERMINAL

7 CONTROL IN / OUT

Use for connecting to other Pioneer components bearing the Pioneer mark. Connect the CONTROL OUT of one component to the CONTROL IN of another using a mini-plug cord. The device at the beginning of the chain acts as the remote control sensor for everything in the chain.

8 VHF/UHF IN

Connect the TV antenna here

9 VHF/UHF OUT

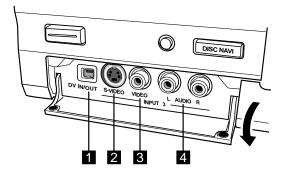
Passes the signal from the VHF/UHF IN to your TV/monitor

10 AUDIO/VIDEO INPUT 1, 2/AUTO REC

For recording from a camcorder, VCR, satellite receiver or other equipment

11 AUDIO/VIDEO OUTPUT 1, 2

For connecting to the audio and video inputs of a TV, monitor, AV receiver or other equipment



1 DV IN/OUT jack

A combined input and output jack for connecting a digital camcorder. See page 19 for details.

2 S-VIDEO input (INPUT 3)

Connect to an S-Video output of an external component.

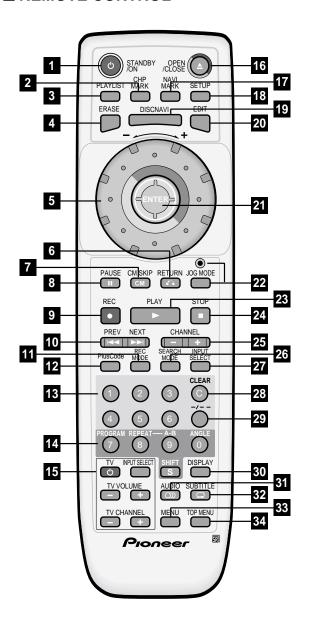
3 VIDEO input (INPUT 3)

Connect to a composite (standard) video output of an external component.

4 AUDIO L/R (INPUT 3)

Connect to a stereo pair of audio outputs of an external component.

■ REMOTE CONTROL



1 U STANDBY/ON

Switches the recorder on/into standby

2 CHP MARK

Inserts a chapter marker when playing/recording a VR mode DVD-RW disc

3 PLAYLIST

Switches beween Original and Playlist

4 ERASE

Shortcut to the erase function in the Discnavi or Title List screen

5 Jog dial

Controls scanning/slow motion speed and direction, and frame advance/reverse

6 € RETURN

Returns to the previously displayed on-screen display

7 CM SKIP

Skips 30 seconds forward on the disc (about the length of a typical TV commercial)

8 II PAUSE

Pauses playback or recording

9 ● REC

Starts recording. Press repeatedly to set the recording time

10 **I**◄ PREV

Track or chapter skip/displays the previous page of a menu

▶►I NEXT

Track or chapter skip/displays the next page of a menu

11 REC MODE

Switches the recording mode between SP to MN for a VR mode disc, or between V1 and V2 for a Video mode disc

12 PlusCode (G-code for LB type)

Press, then use the number buttons to enter a PlusCode(G-code for LB type) programming number for timer recording

13 Number buttons

14 PROGRAM (Press SHIFT first to access)

Displays the program play screen

REPEAT (Press SHIFT first to access)

Selects the repeat play mode

A-B (Press SHIFT first to access)

Marks a loop for looped playback

ANGLE (Press SHIFT first to access)

Switches camera angles on discs with multi-angle scenes

SHIFT

Press first to access the above functions

15 TV controls

Use this remote to control your TV

16 ▲ OPEN/CLOSE

Opens/closes the disc tray

17 NAVI MARK

Selects a thumbnail picture for the current title for use in the Discnavi screen

18 SETUP

Displays the Setup menu

19 DISCNAVI

Displays the Discnavi screen

20 EDIT

Shortcut to the editing functions within the Discnavi or Title List screen

21 Joystick / ENTER

Use the joystick to navigate all on-screen displays. Press ENTER to select the currently highlighted option.

22 JOG MODE button and indicator

Switches the Jog dial between scanning and frame advance mode

23 ► PLAY

Starts playback

24 ■ STOP

Stops playback/recording

25 CHANNEL -/+

Changes the channel of the built-in TV tuner

26 SEARCH MODE

Allows searching of the disc by title, chapter, track, time, etc.

27 INPUT SELECT

Changes the input to use for recording

28 CLEAR

Clears the current setting, etc.

29 -/---

Press, then use the number button to enter a twodigit channel number

30 DISPLAY

Displays/changes the on-screen information displays

31 AUDIO

Changes the audio language or channel

32 SUBTITLE

Displays/changes the subtitles included in multilingual DVD-Video discs

33 MENU

Displays the disc menu of DVD-Video discs or the Title List screen of Video mode DVD-R/RW discs

34 TOP MENU

Displays the disc 'top' menu of DVD-Video discs or the Title List screen of Video mode DVD-R/RW discs

8.2 SPECIFICATIONS

General
System
Recording
Recording format
Recordable discs
Video recording format Sampling frequency
Tuner Receivable channels VHF 1–13ch UHF 14–69ch CATV C1–C125ch
Timer Programs

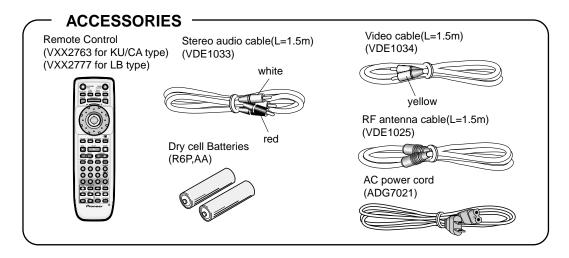
Input/Output

Πρανοαιραι
VHF/UHF antanna input/output terminal VHF/UHF set
75 Ω (F-shape connector)
Video input Input 1,2 (rear), 3 (front)
Input level 1 Vp-p (75 Ω)
Jacks RCA jack
Video output Output 1,2
Output level
Jacks RCA jack
S-Video input
Y (luminance) - Input level 1 Vp-p (75 Ω)
C (color) - Input level
Jacks
S-Video output Output 1,2
Y (luminance) - Output level 1 Vp-p (75 Ω)
C (color) - Output level
Jacks 4 pin mini DIN
Component video output
Output level Y: 1.0 Vp-p (75 Ω)
P _B , P _R : 0.7 Vp-p (75 Ω)
Jacks RCA jacks
Audio input Input 1,2 (rear), 3 (front) L/R
Input level
During audio input2V rms
(Input impedence: more than 22kΩ)
Jacks RCA jacks
Audio output
During audio output2V rms
(Output impedence: less than 1.5kΩ)
Jacks RCA jacks
Control input/output Mini jack 1 each
DV input/output 4 pin (i.LINK/IEEE 1394 standard)

Supplied accessories

Remote control	. 1
Dry cell batteries (AA/R6P)	2
Stereo audio cable (red/white)	. 1
Video cable (yellow)	. 1
RF antenna cable	
Power cable	. 1
DVD-RW disc (KU/CA type only)	. 1
Operating Instructions (for KU/CA type)	. 1
Operating Instructions (for LB type)	2
Warranty card (KU/CA type only)	. 1

Note: The specifications and design of this product are subject to change without notice, due to improvement.





Service Manual



ORDER NO. RRV2423

DVD-R/RW CD-R/RW WRITER DVD-R/RW CD-R/RW WRITER

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

	Туре	Model	Power Requirement	Remarks		
	- 7,50	DVR-A03		Kemarks		
	KB	0	DC Power supply from other system			

NECESSARY INFORMATION FOR DHHS RULES MARKED ON THE TOP COVER BELOW:

DANGER – VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN. AVOID DIRECT EXPOSURE TO BEAM.

CONTENTS

1. SAFETY INFORMATION ······ 2	7. GENERAL INFORMATION 52
2. EXPLODED VIEWS AND PARTS LIST 4	7.1 DIAGNOSIS 52
3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM 8	7.1 DISASSEMBLY 52
4. PCB CONNECTION DIAGRAM ····· 33	7.2 PARTS 55
5. PCB PARTS LIST 38	7.2.1 IC ····· 55
6. ADJUSTMENT 41	8. PANEL FACILITIES AND SPECIFICATIONS 81

PIONEER CORPORATION 4-1, Meguro 1-chome, Meguro-ku, Tokyo 153-8654, Japan PIONEER ELECTRONICS SERVICE, INC. P.O. Box 1760, Long Beach, CA 90801-1760, U.S.A. PIONEER EUROPE NV Haven 1087, Keetberglaan 1, 9120 Melsele, Belgium PIONEER ELECTRONICS ASIACENTRE PTE. LTD. 253 Allexandra Road, #04-01, Singapore 159936 © PIONEER CORPORATION 2001

1. SAFETY INFORMATION

This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual. Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING

This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to cause cancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 - Proposition 65

VARO! -

AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALTTIINA NÄKYMÄTTÖMÄLLE LASERSÄTEIYLLE. ÄLÄ KATSO SÄTEESEEN.

[ADVARSEL: -

USYNLIG LASERSTRÅLING VED ÅBNING NÅR SIKKERHED SAFBRYDERE ER UDE AF FUNKTION. UNDGÅ UDSÆTTELSE FOR STRÅLING.

VARNING! -

OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD. BETRAKTA EJ STRÅLEN.



LASER kuva 1 Lasersateilyn varoitusmerkki WARNING!

DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.



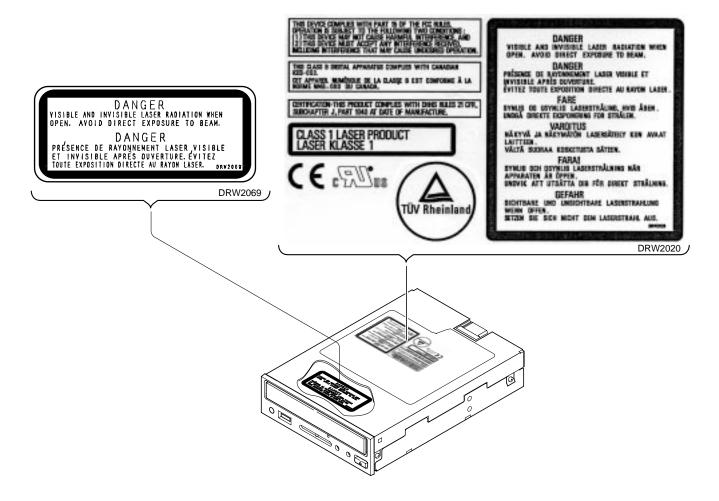
LASER
Picture 1
Warning sign for laser radiation

— IMPORTANT —

THIS PIONNER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

LASER DIODE CHARACTERISTICS — MAXIMUM OUTPUT POWER : 35 mw WAVELENGTH : 658 nm

■ LABEL CHECK



Additional Laser Caution

- The ON/OFF(ON:low level,OFF:high level) status of the CLAMP signals for detcting the loading state are detected by the drive CPUs, and the design prevents laser diode oscillation when the CLAMP signal turns OFF.

 In normal operation, if no disc is clamped, the laser diode oscillation is disabled.

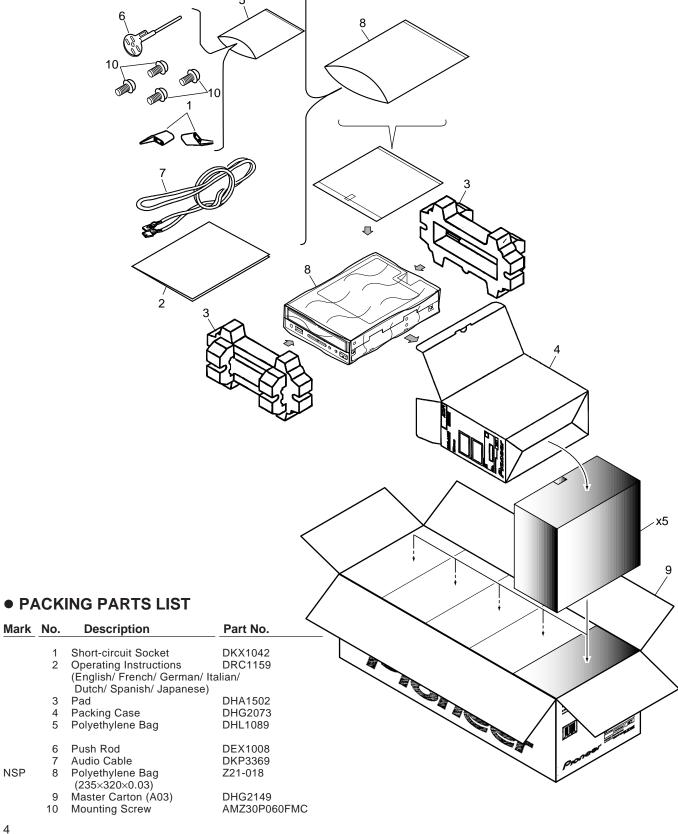
 However, the interlock does not always operate in the test mode. *
- When the cover is opened, close viewing of the objective lens with the naked eye will cause exposure to a Class 3A laser beam.

^{*} Refer to pages 43.

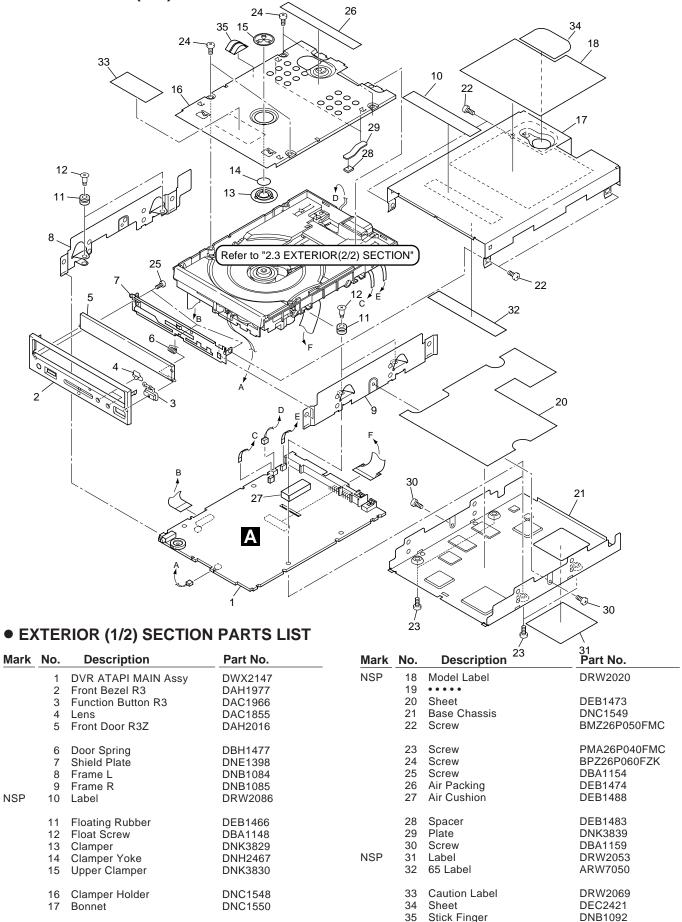
2. EXPLODED VIEWS AND PARTS LIST

- NOTES: ullet Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List. ullet The Δ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
 - Screws adjacent to ▼ mark on the product are used for disassembly.

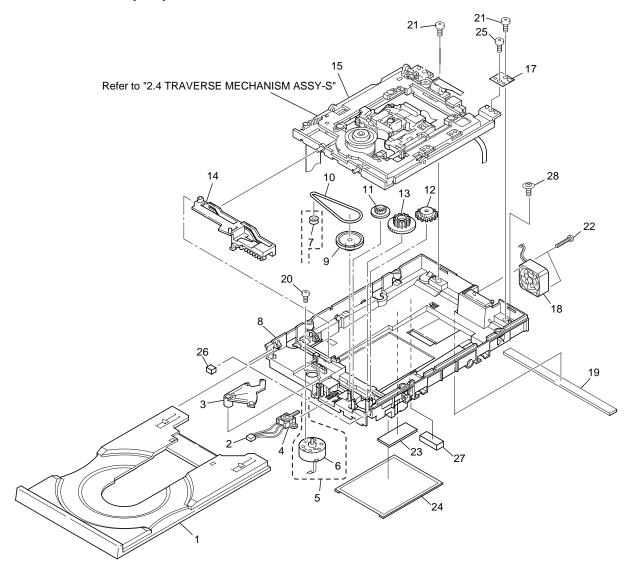
2.1 PACKING



2.2 EXTERIOR (1/2) SECTION 35 15



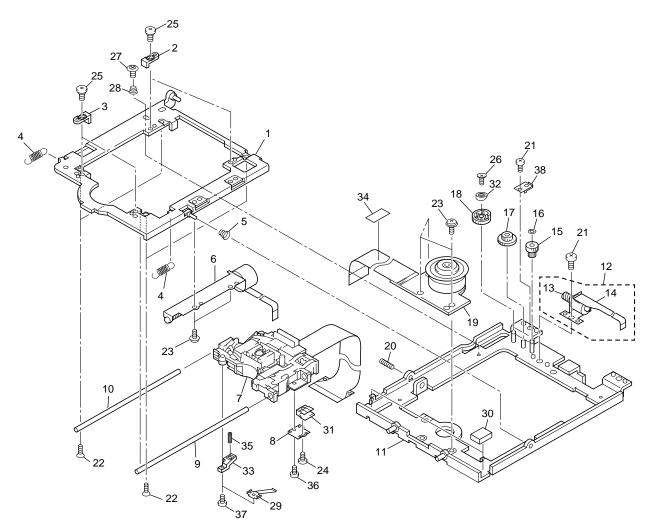
2.3 EXTERIOR (2/2) SECTION



• EXTERIOR (2/2) SECTION PARTS LIST

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	Tray	DNK3812		16	• • • • •	
	2	Connector Assy (3P)	DKP3544		17	Plate	DBK1208
	3	Eject Lever	DNK3817		18	Fan Motor (25mm)	DXM1123
	4	S Lever Switch	DSK1001		19	Packing	DEB1474
	5	Loading Motor Assy	DXX2491		20	Screw	JGZ17P030FMC
NSP	6	Carriage Motor	RXM1090		21	Screw	BPZ26P060FZK
	7	Motor Pulley	PNW1634		22	Screw (2.6×16)	DBA1153
	8	Loading Base	DNK3811		23	Air Cushion	DEB1488
	9	Gear Pulley	DNK3813		24	Sheet (Rubber)	DEC2411
	10	Rubber Belt	DEB1465		25	Screw	BMZ26P060FMC
	11	Gear A	DNK3814		26	Spacer POR (T5)	DEB1485
	12	Gear C	DNK3816		27	Spacer	DEB1482
	13	Gear B	DNK3815		28	Screw	VBA1034
	14	Clamp Cam	DNK3818				
	15	Traverse Mechanism Assy-S	DXX2498				

2.4 TRAVERSE MECHANISM ASSY-S

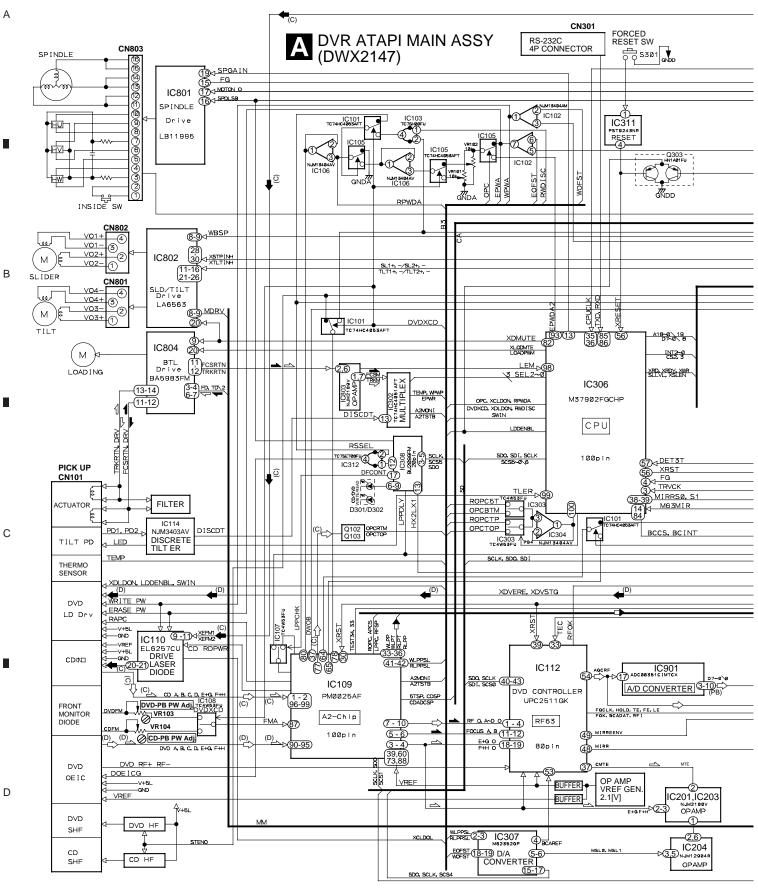


• TRAVERSE MECHANISM ASSY-S PARTS LIST

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	Tilt Base	DNH2466		21	Screw	BMZ26P040FMC
	2	Stopper R	DEB1469		22	Screw	CMZ20P050FMC
	3	Stopper F	DEB1471		23	Screw	PMA20P040FMC
	4	Tilt Spring Y	DBH1479		24	Screw	DBA1121
	5	Tilt Spring X	DBH1478		25	Screw	DBA1149
	6	Stepping Motor	DXM1151		26	Tilt Screw	DBA1157
NSP	7	Pickup Assy	OWY8001		27	Shoulder	DBA1158
	8	Joint Spring	DBK1196		28	Tilt Spring Z	DBH1482
	9	Main Shaft	DLA1921		29	Guide Spring	DBK1195
	10	Sub Shaft	DLA1923		30	Cushion	DEB1484
	11	Mecha Base	DNH2465	NSP	31	Guide Blade	DNK3721
	12	Tilt Motor Assy	DXX2492		32	Cam Cover	DNK3863
	13	Worm	DNK3825		33	Sub Guide	DNS1217
	14	Tilt Motor	DXM1152	NSP	34	Acetate Tape(F)	REH1008
	15	Tilt Gear A	DNK3826		35	TAN Screw	VNL1761
	16	Washer	WT21D040D050		36	Screw	PBZ20P040FMC
	17	Tilt Gear B	DNK3827		37	Screw	PBZ20P060FMC
	18	Tilt Cam	DNK3828		38	Hold Plate	DBK1198
	19	Spindle Motor	DXM1150				
	20	Screw	ZMR30H080FZK				

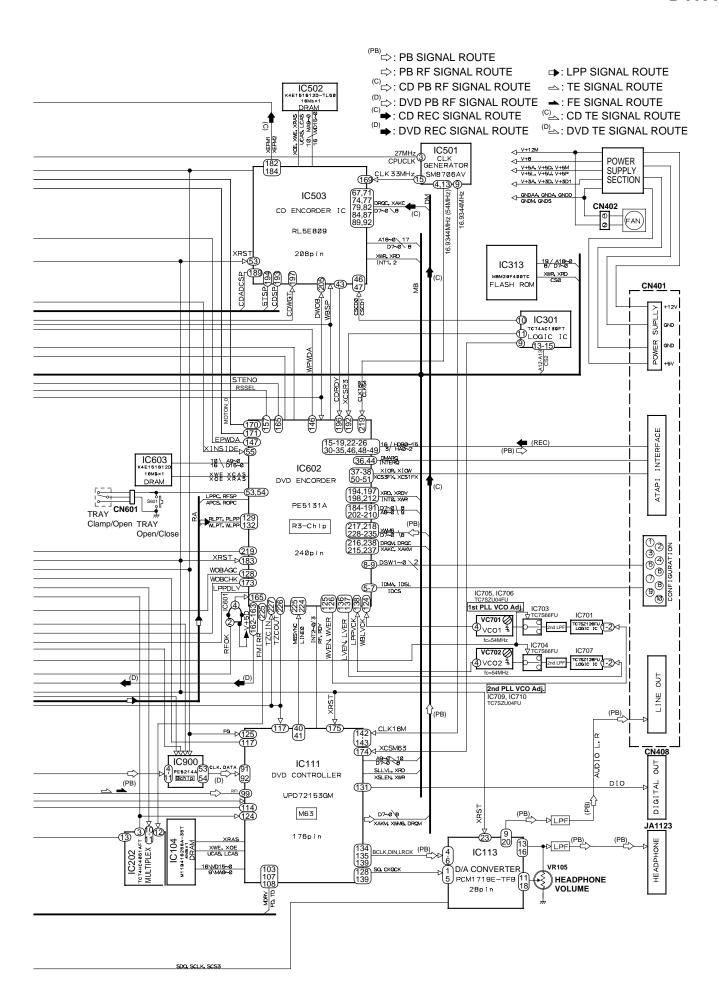
3. BLOCKDIAGRAM AND SCHEMATIC DIAGRAM

3.1 BLOCK DIAGRAM



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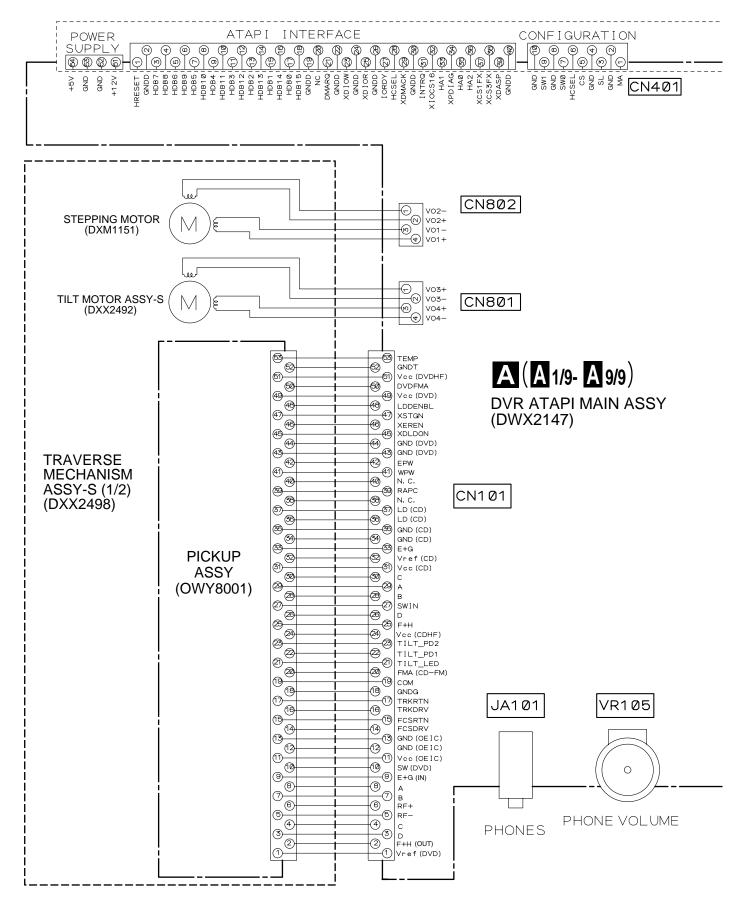
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3.2 OVERALL WIRING DIAGRAM



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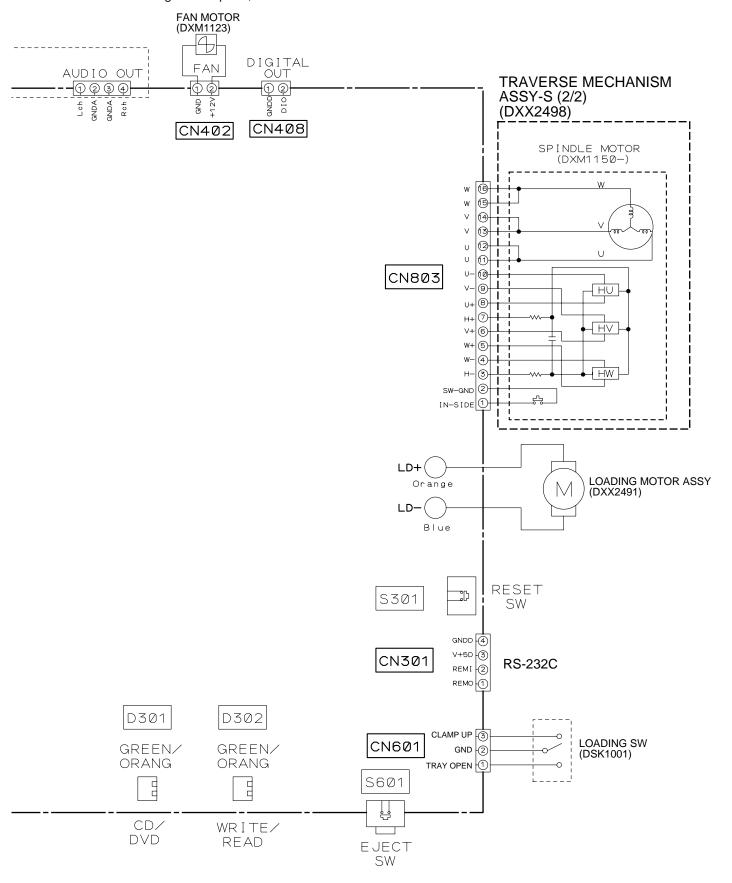
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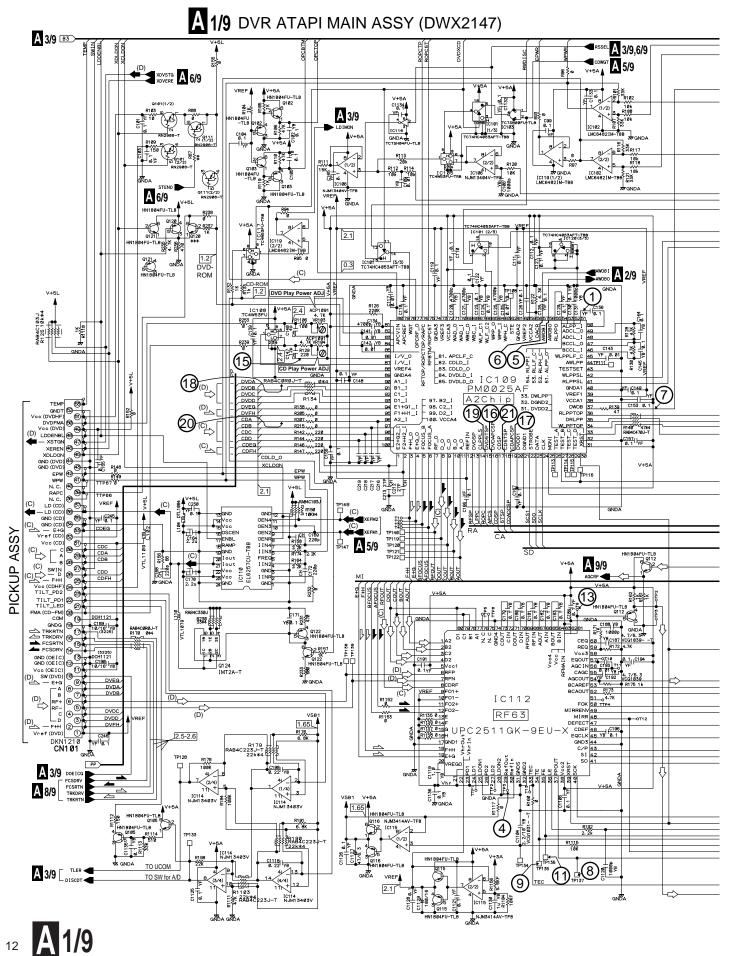
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Note: When ordering service parts, be sure to refer to "EXPLODED VIEWS and PARTS LIST" or "PCB PARTS LIST".

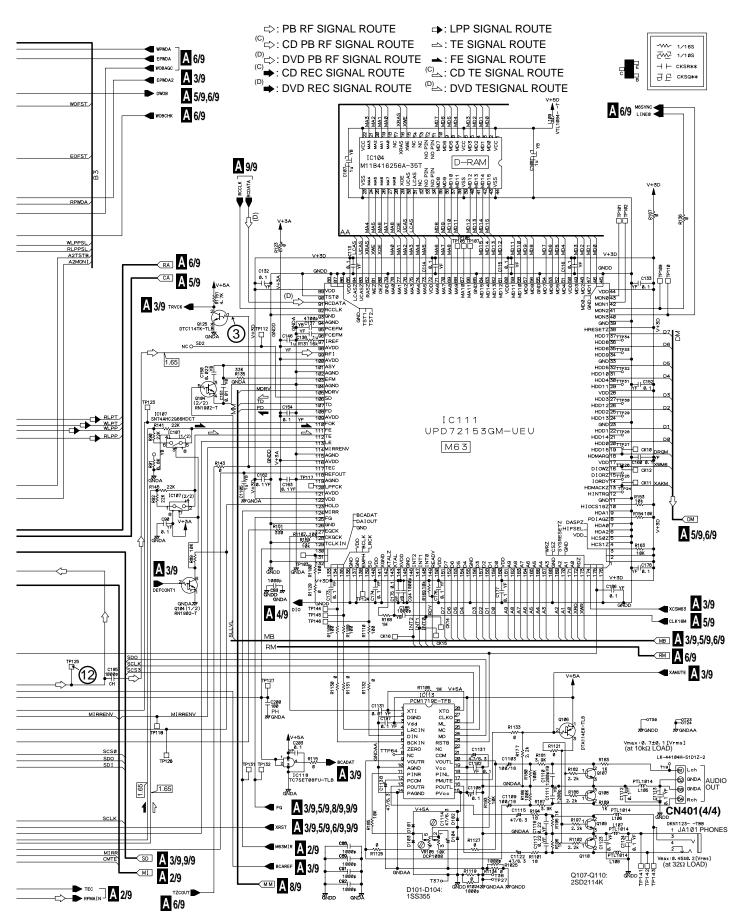


3.3 DVR ATAPI MAIN ASSY (1/9)



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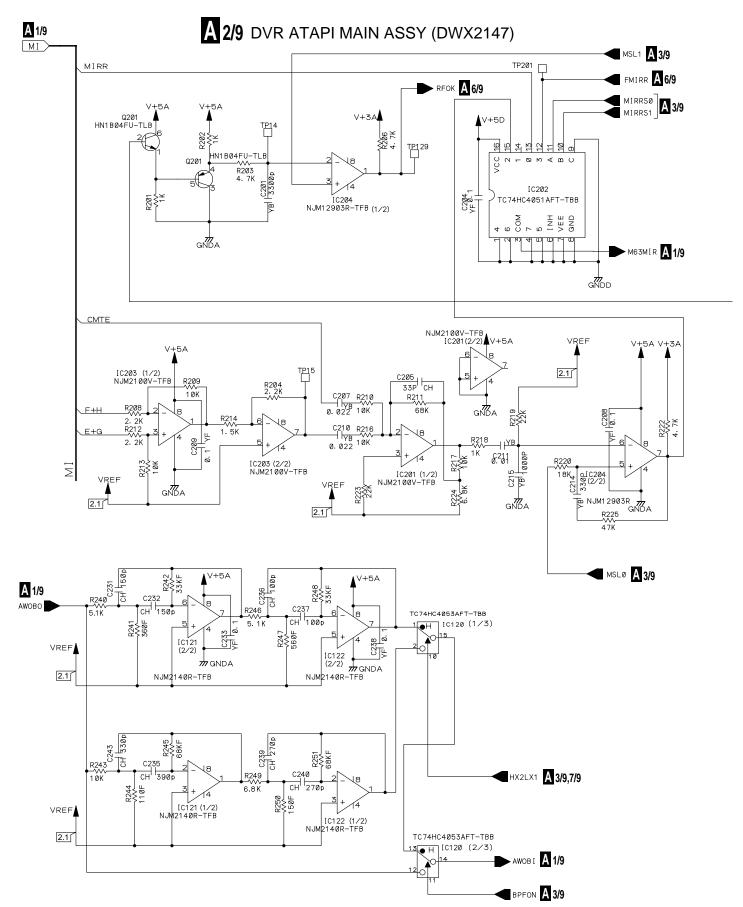
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3.4 DVR ATAPI MAIN ASSY (2/9)



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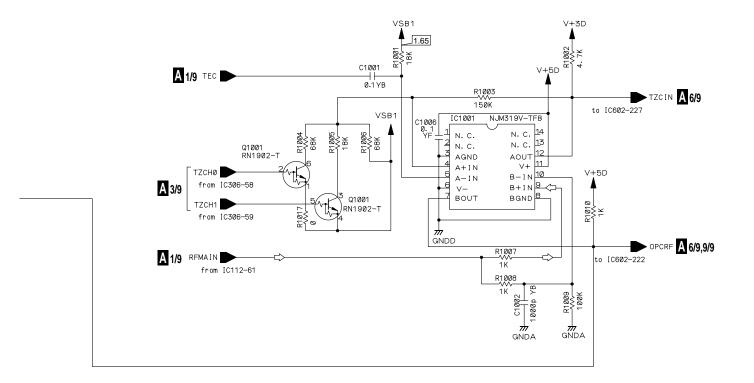
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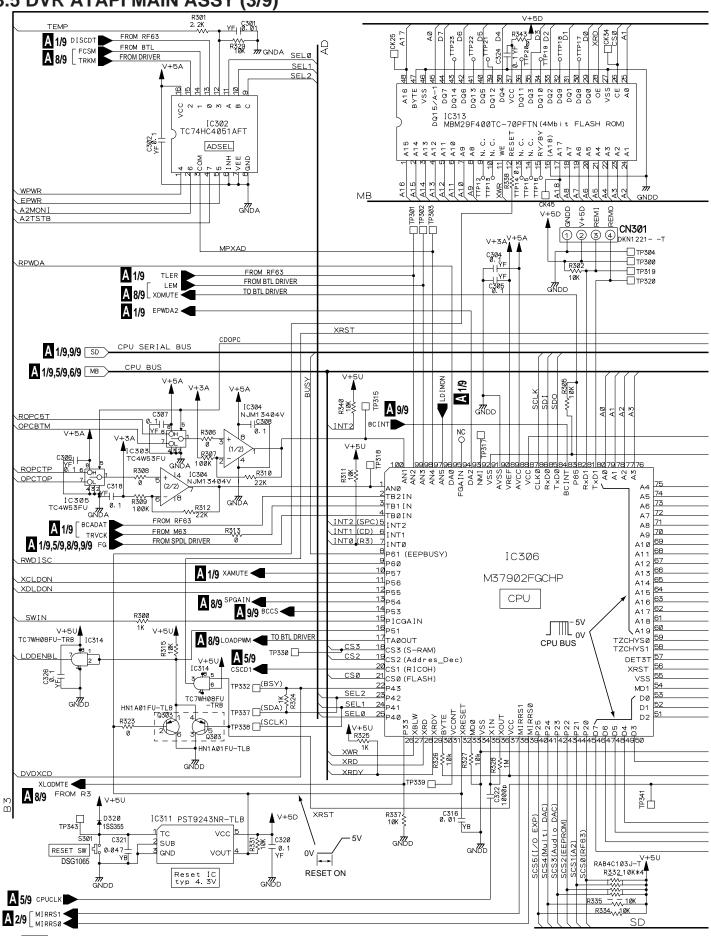
A 2/9 15

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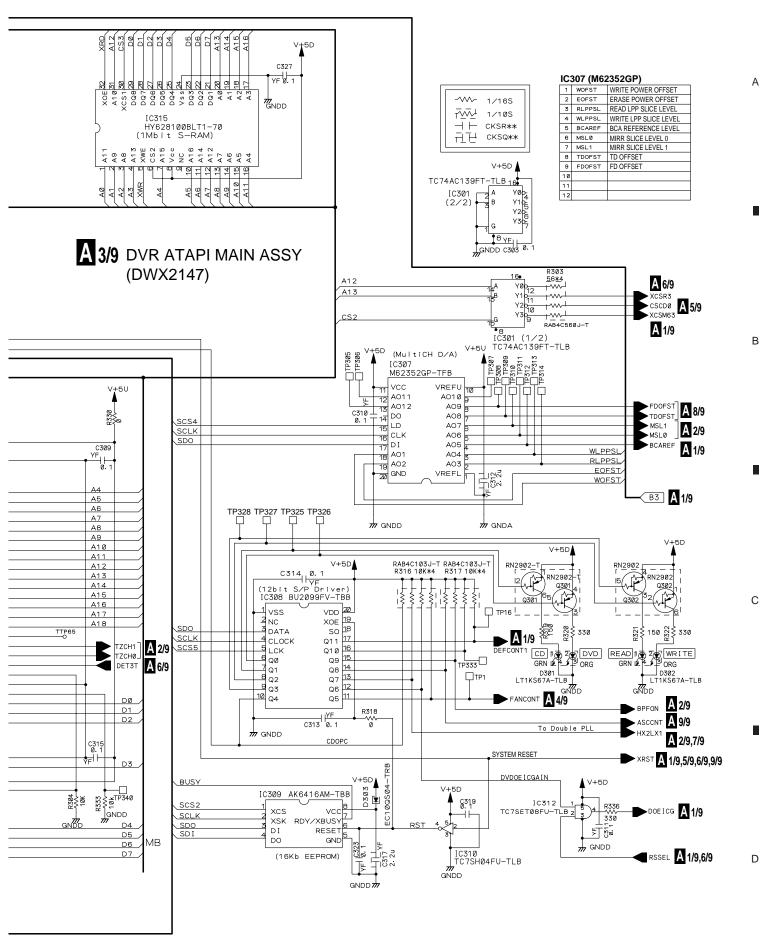
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3.5 DVR ATAPI MAIN ASSY (3/9)



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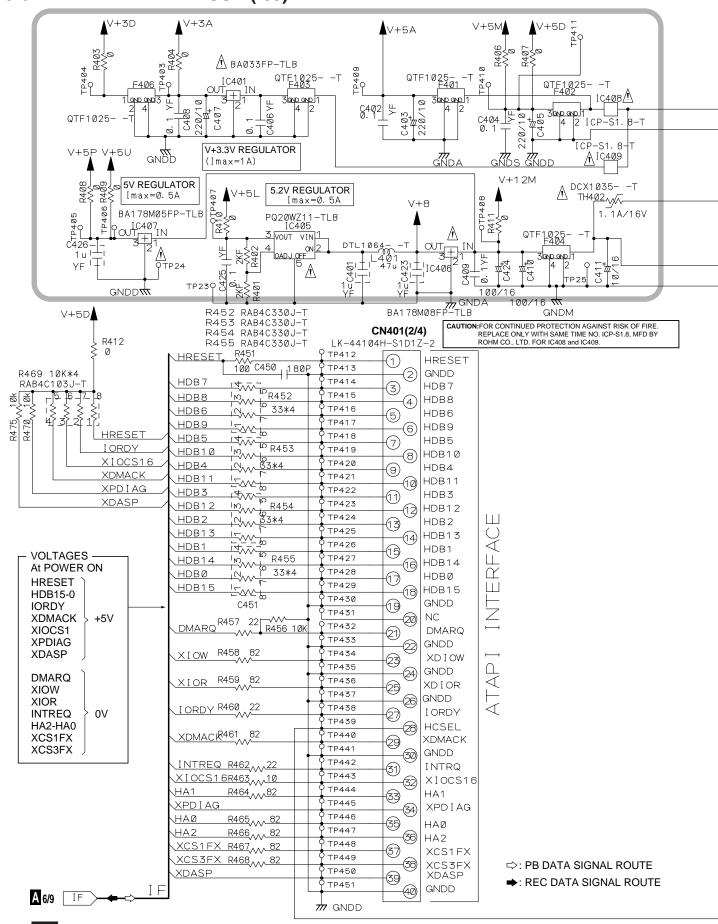
A 3/9 17

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3.6 DVR ATAPI MAIN ASSY (4/9)

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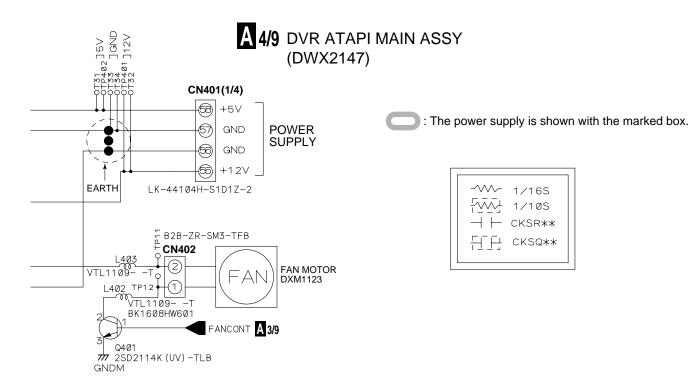
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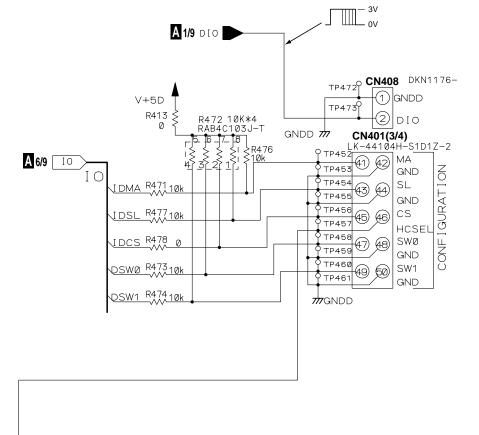
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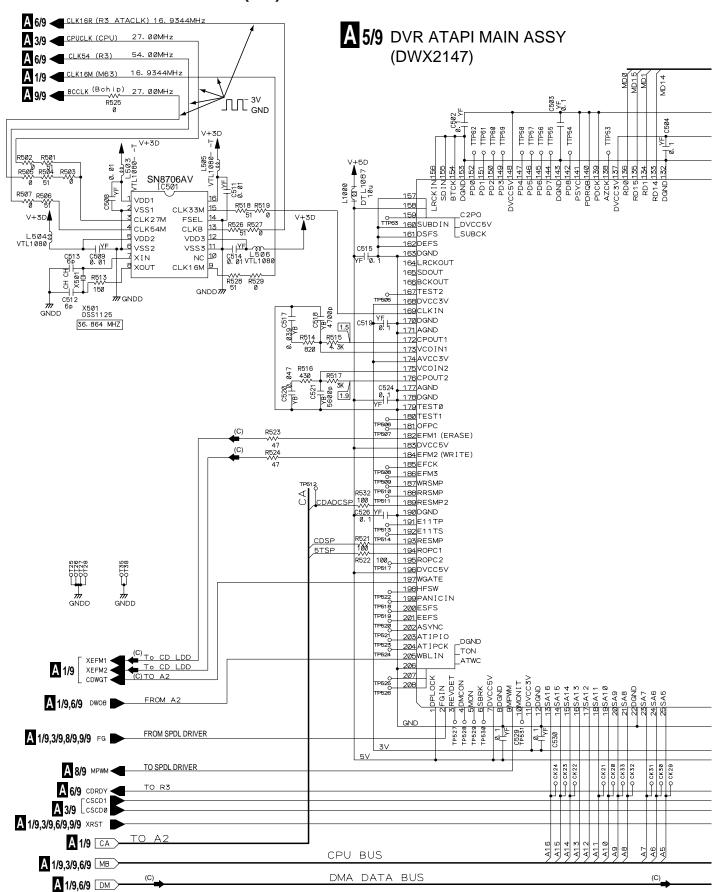


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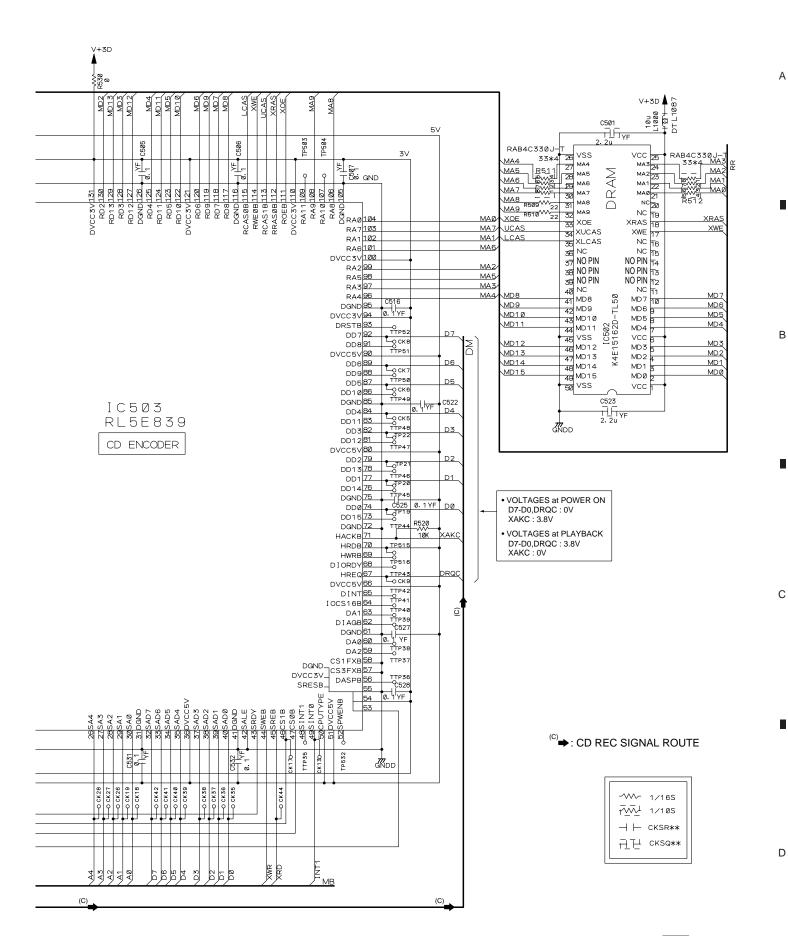
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3.7 DVR ATAPI MAIN ASSY (5/9)

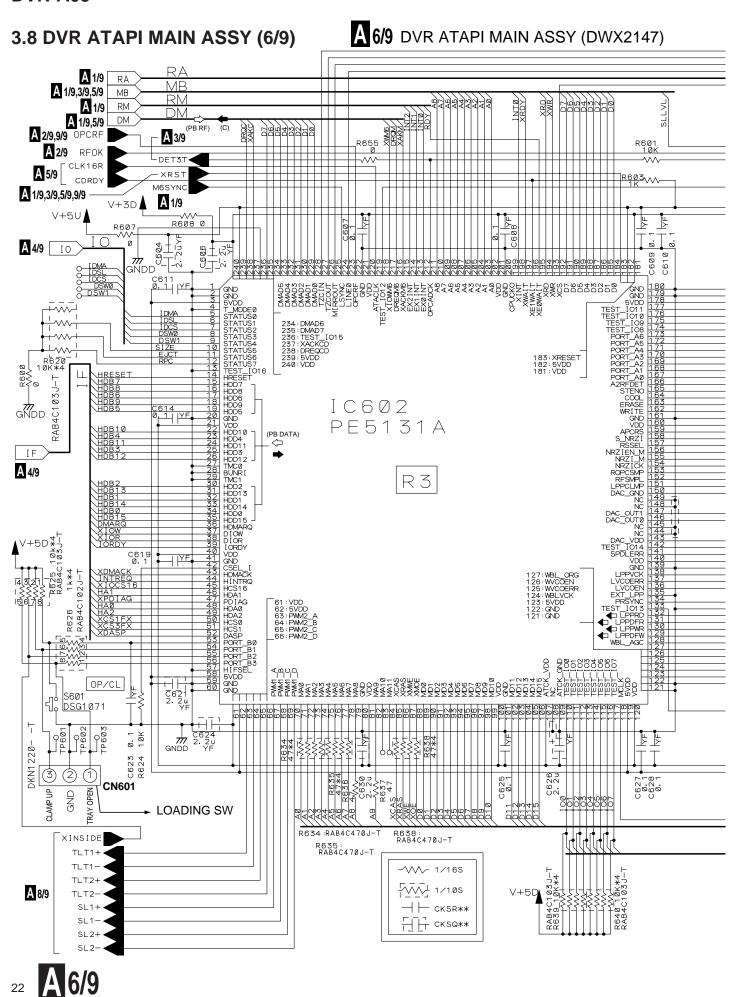


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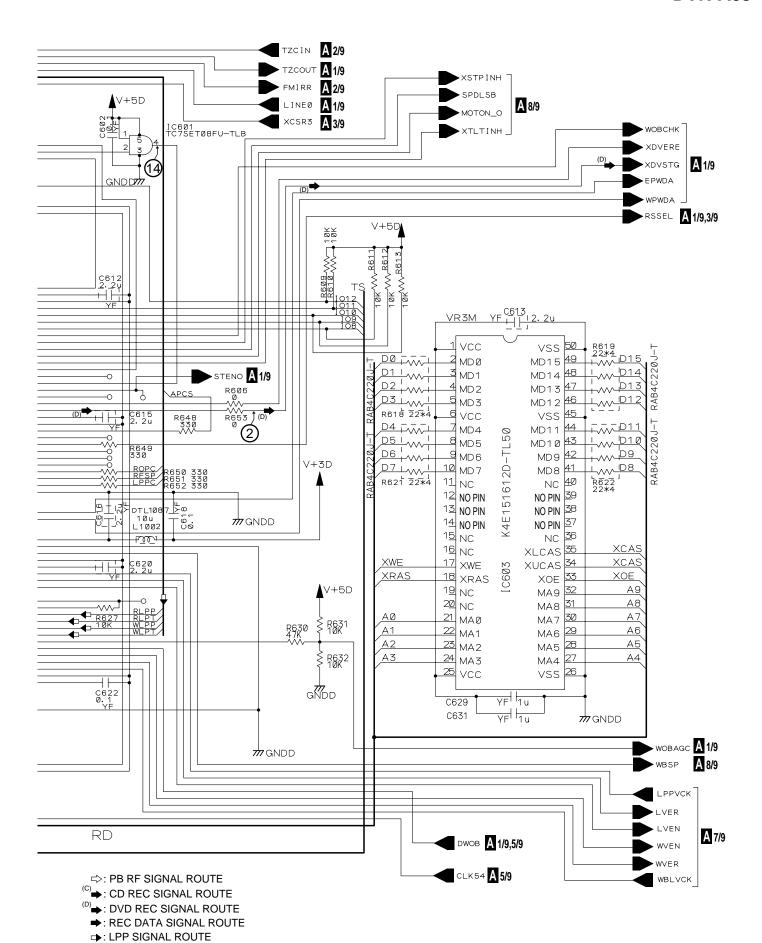
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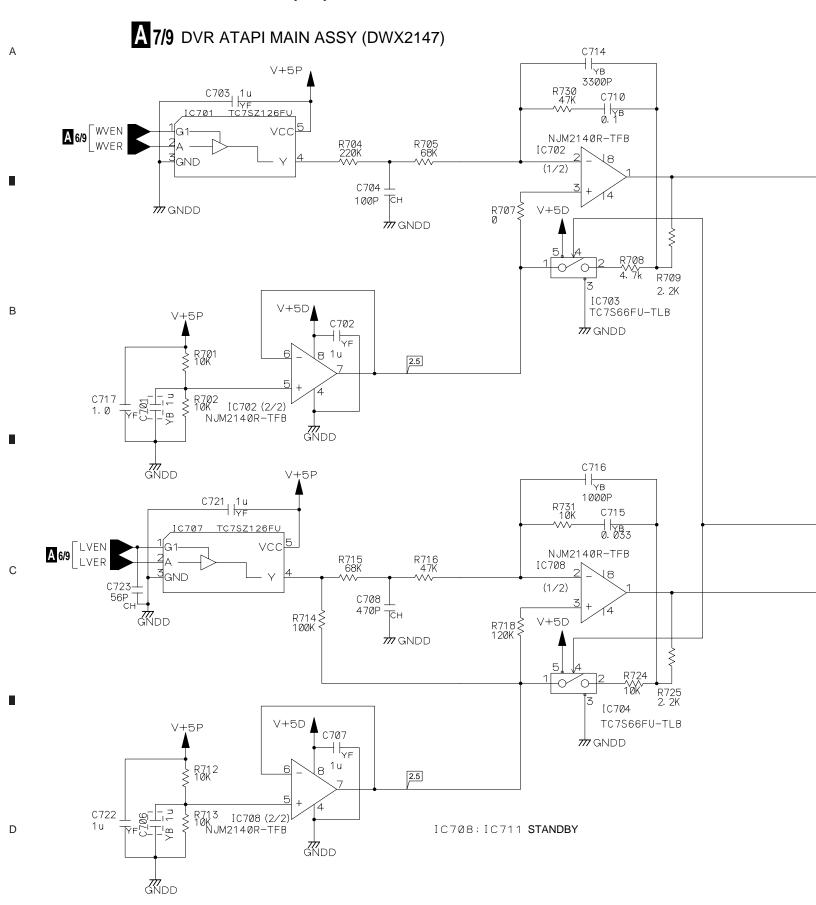
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3.9 DVR ATAPI MAIN ASSY (7/9)



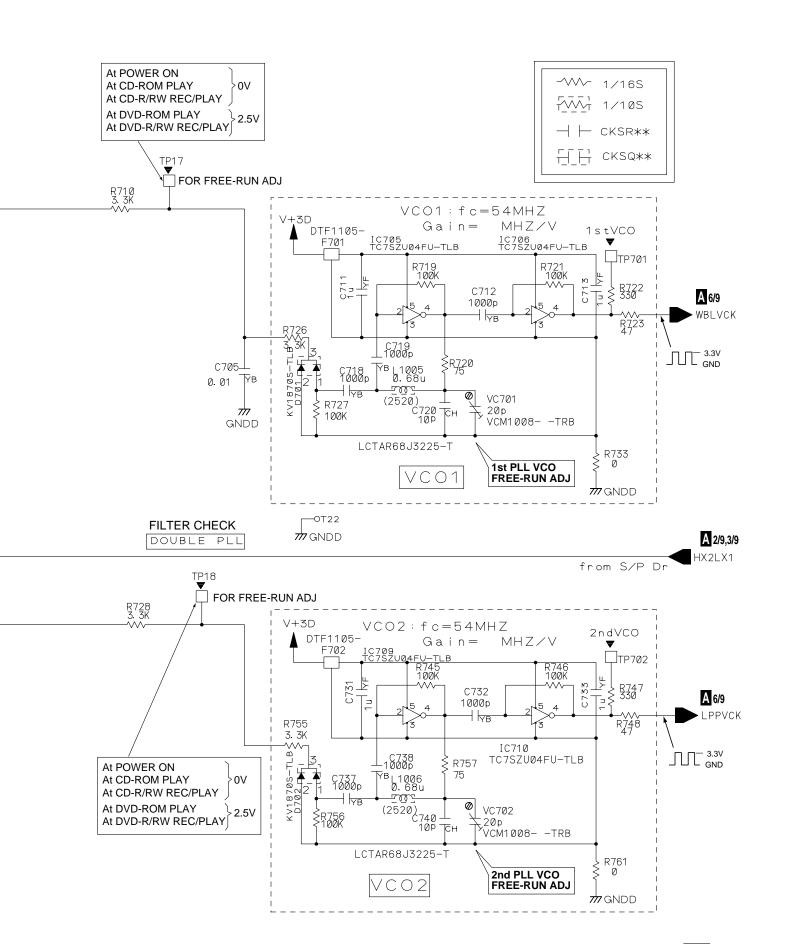
A 7/9

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A 7/9 25

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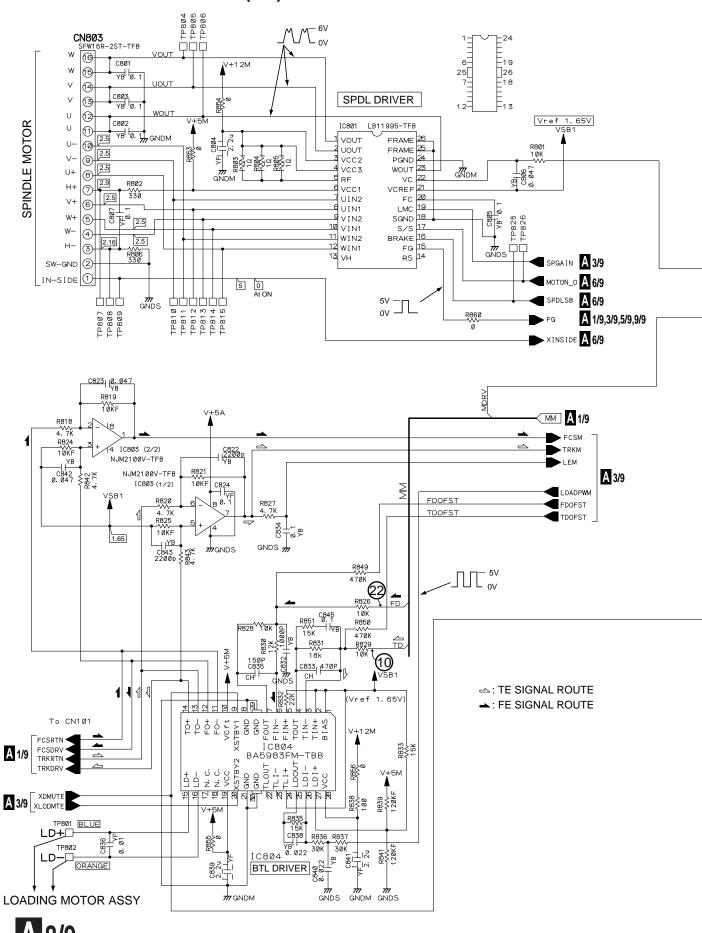
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3.10 DVR ATAPI MAIN ASSY (8/9)

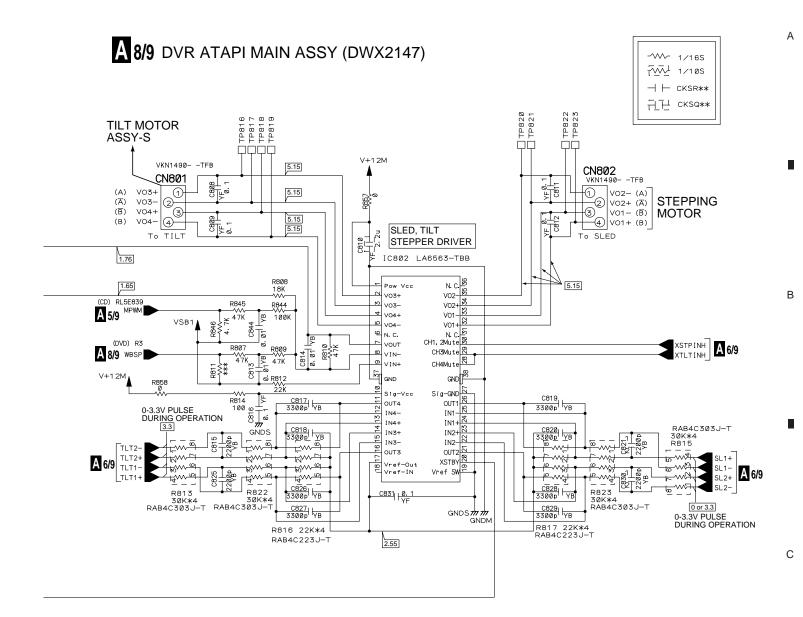
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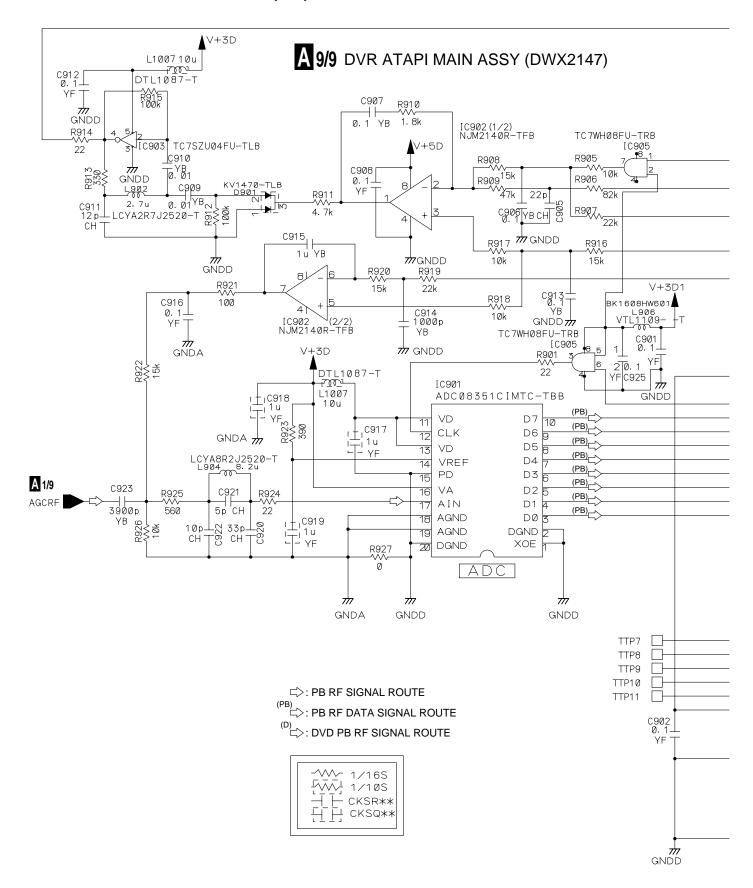
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3.11 DVR ATAPI MAIN ASSY (9/9)

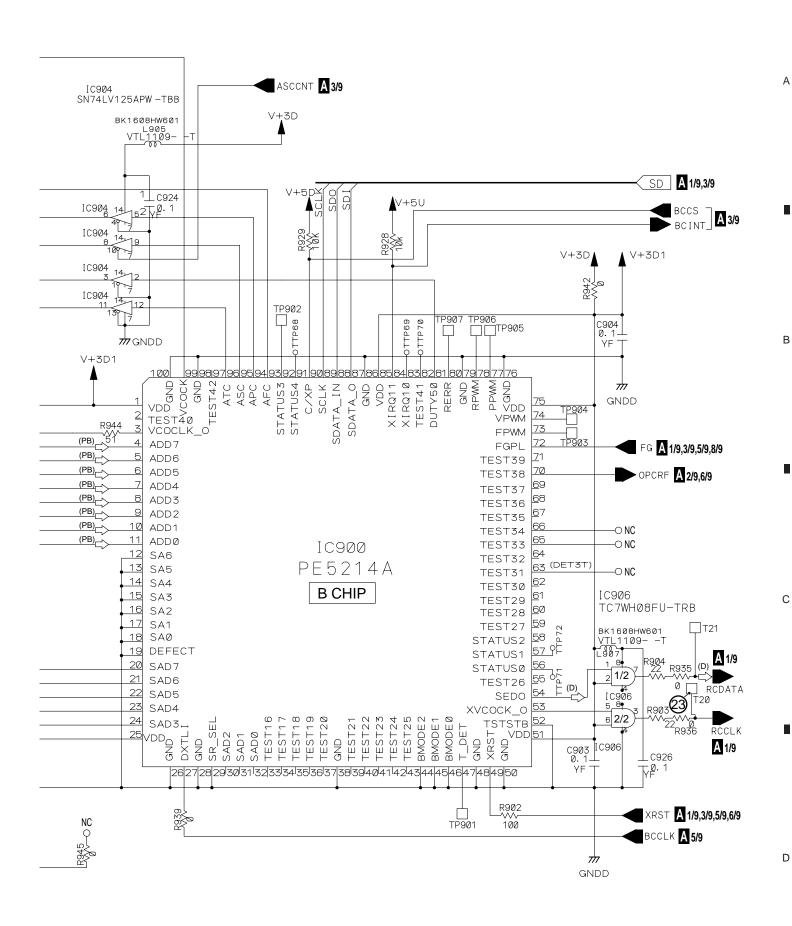


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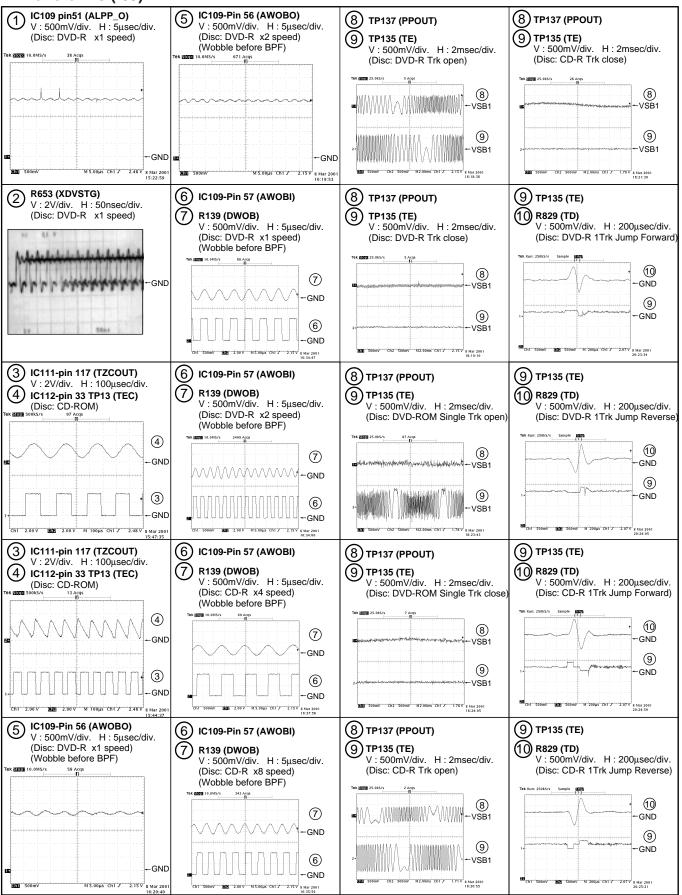
A 9/9

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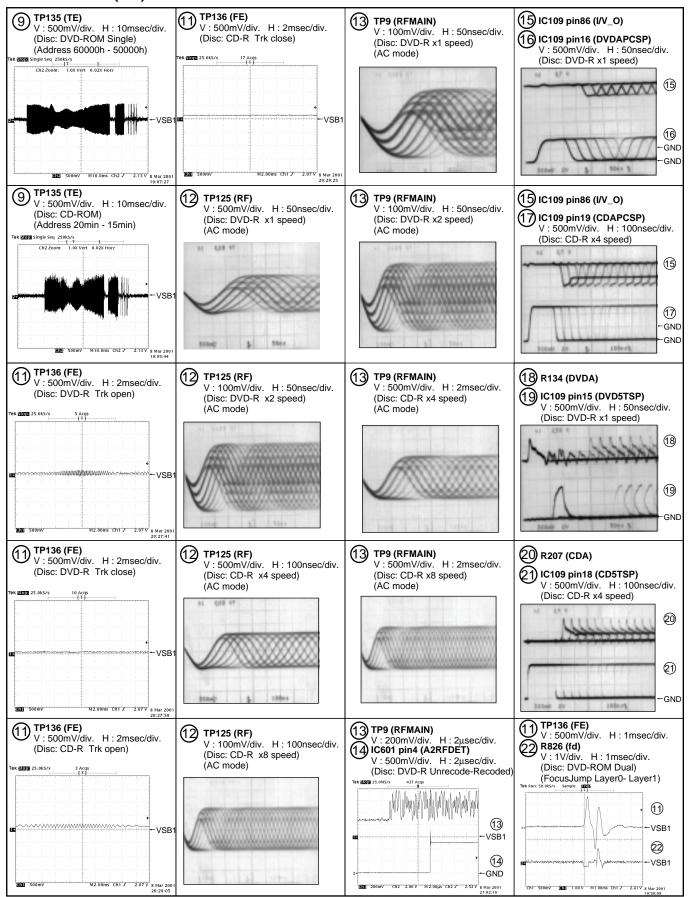
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Waveforms (1/3)

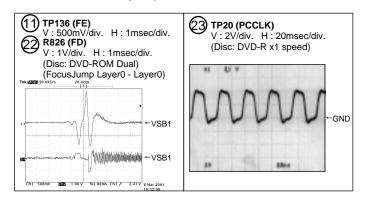


Waveforms (2/3)



DVR-A03

● Waveforms (3/3)



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4. PCB CONNECTION DIAGRAM

NOTE FOR PCB DIAGRAMS:

- 1. Part numbers in PCB diagrams match those in the schematic diagrams.
- 2. A comparison between the main parts of PCB and schematic diagrams is shown below.

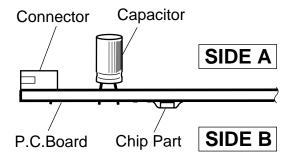
Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name
(0 0 0 B C E	B B C C C C C C C C C C C C C C C C C C	Transistor
•(0 0 0) B C E	B O	Transistor with resistor
000 DGS		Field effect transistor
@00\\\	***************************************	Resistor array
000		3-terminal regulator

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- 3. The parts mounted on this PCB include all necessary parts for several destinations.
 - For further information for respective destinations, be sure to check with the schematic diagram.
- 4. View point of PCB diagrams.

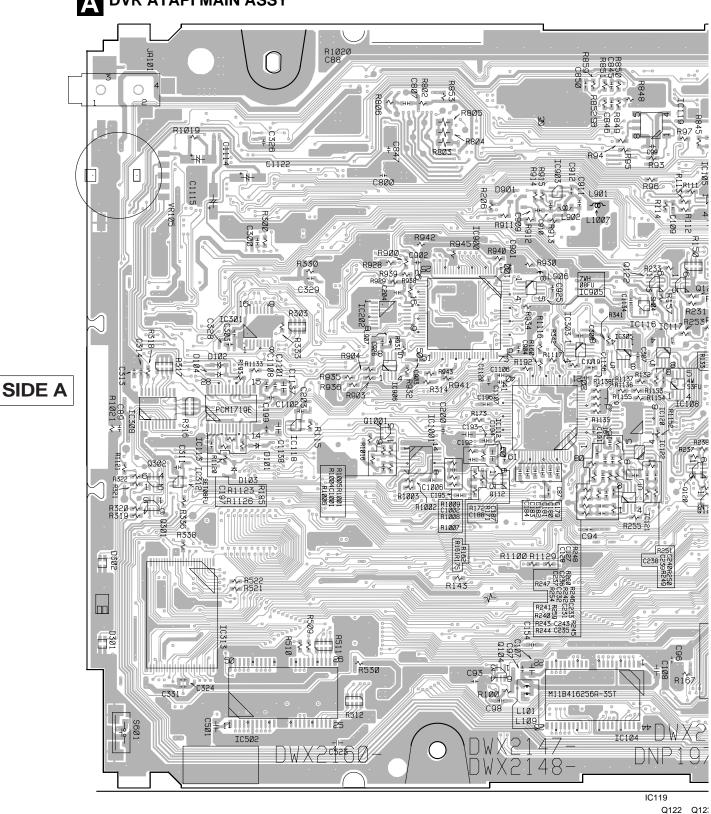
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• This PCB is a four-layered board.

4.1 DVR ATAPI MAIN ASSY

A DVR ATAPI MAIN ASSY

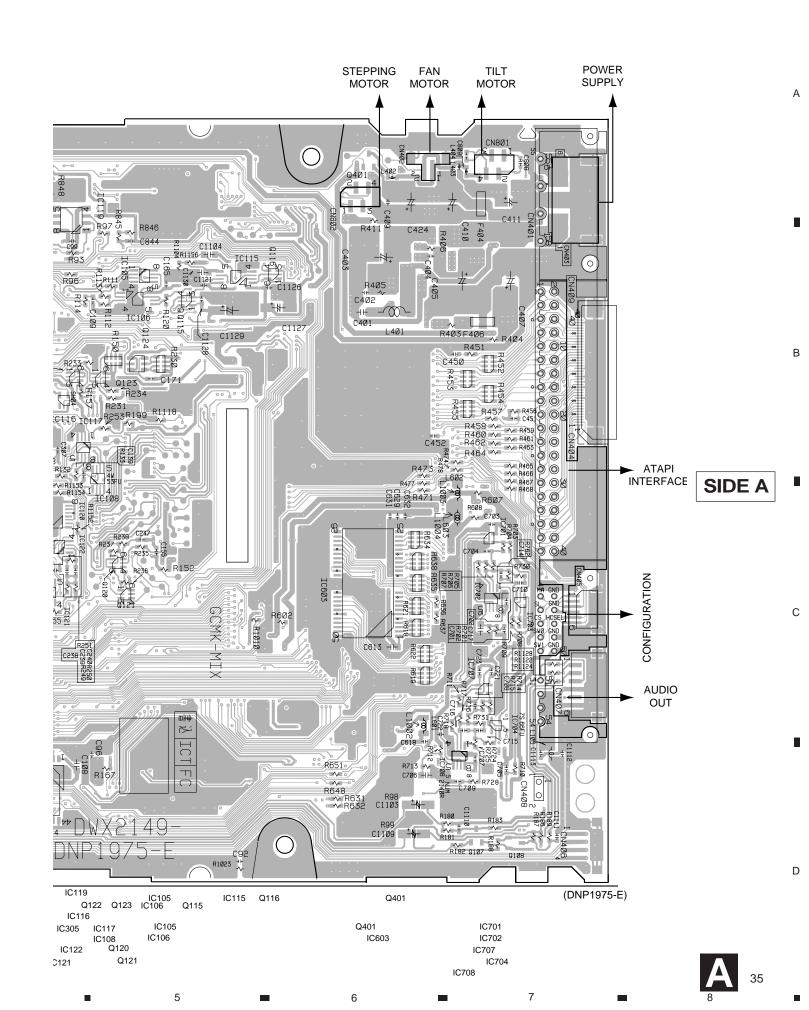


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IC900 IC903 IC303 IC305 IC117 IC306 IC906 IC905 Q112 IC108 IC122 Q302 IC312 IC118 Q1001 IC1001 IC112 Q104 IC121 IC313 IC104 IC502

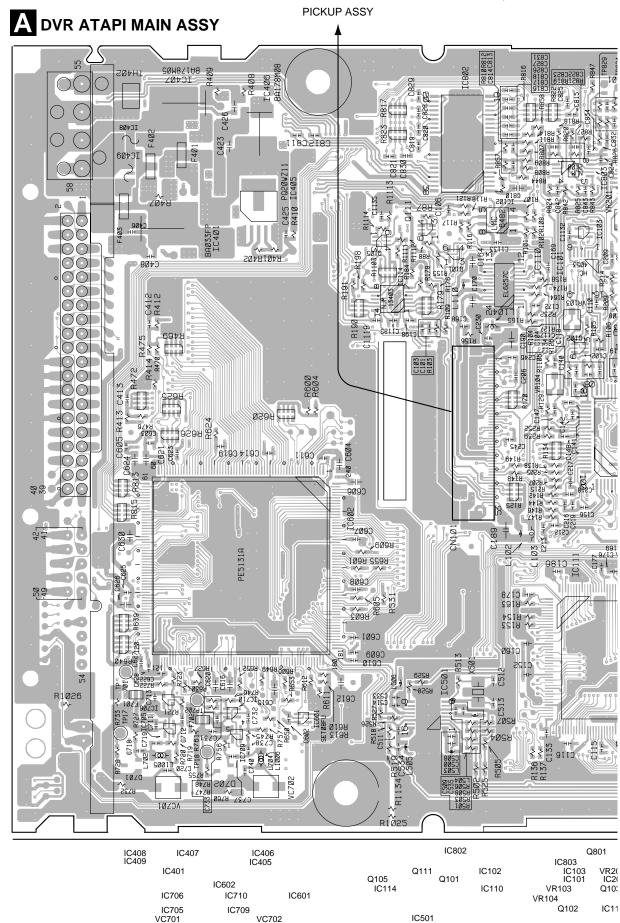
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IC116



DVR-A03

This PCB is a four-layered board.



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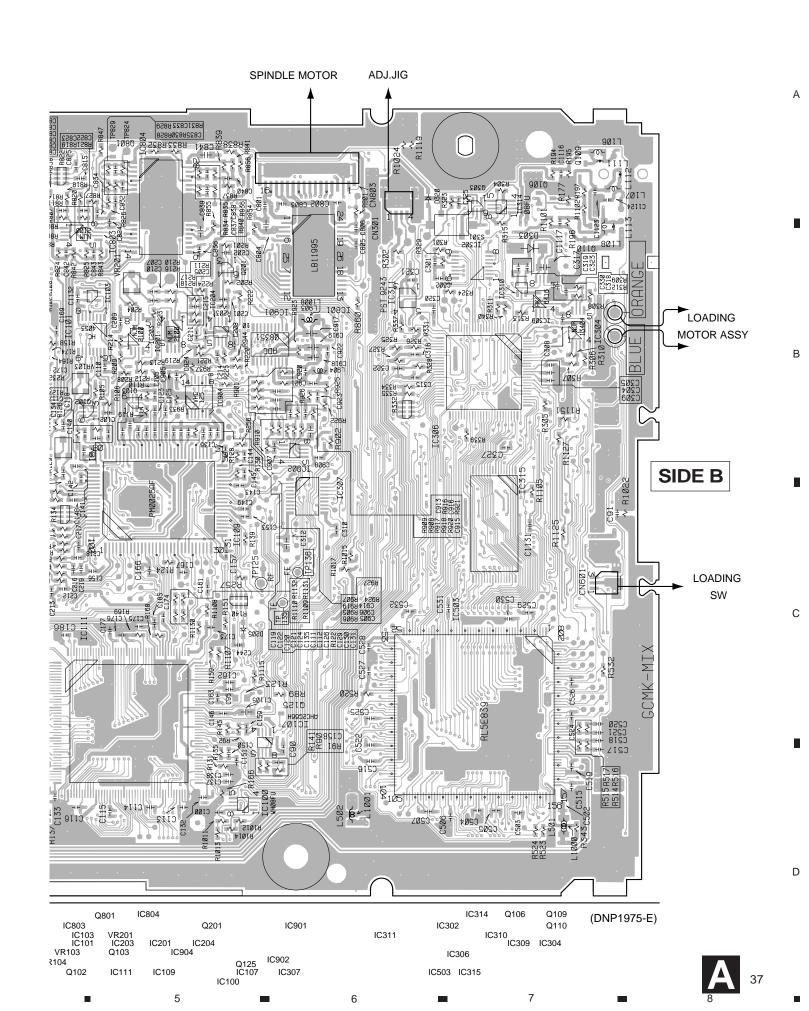
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SIDE B

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5. PCB PARTS LIST

NOTES: • Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.

- The \triangle mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- When ordering resistors, first convert resistance values into code form as shown in the following examples.
 Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
LIST		ASSEMBLIES ATAPI MAIN ASSY	DWX2147		IC101, IC703,	IC302 IC120 IC704 IC312, IC601	TC74AC139FT TC74HC4051AFT TC74HC4053AFT TC7S66FU TC7SET08FU
A	DVR	ATAPI MAIN ASSY			IC103 IC116,	IC310	TC7SH00FU TC7SH04FU
SEMI	COND	UCTORS			IC701,	IC707	TC7SZ126FU
^	IC901 IC309 IC401)	ADC08351CIMTC AK6416AM BA033FP			IC706, IC709, IC710, IC903 IC905, IC906	TC7SZU04FU TC7WH08FU UPC2511GK-9EU-X
<u>^</u>	IC407 IC406	;	BA178M05FP BA178M08FP		IC111	-Q 110, Q 401	UPD72153GM-UEU 2SD2114K DTA114EK
Δ	IC502	s, s, IC409 (1.8A /50V) s, IC603	BA5983FM BU2099FV HY628100BLT1-70 ICP-S1.8 K4E151612D-TL50		Q 115,	Q 103, Q 105, Q 112 Q 116, Q 121, Q 122, Q 201 1,Q 104	DTC114TK HN1A01FU HN1B04FU HN1B04FU RN1902
	IC802 IC801 IC102 IC104 IC306	e, IC119	LA6563 LB11995-TFB LMC6482IM M11B416256A-35T M37902FGCHP		Q 101, D 101- D 303	Q 302 Q 111 -D 104, D 320	RN2902 RN2906 1SS355 EC10QS04
	IC307 IC313 IC204 IC114 IC106	.	M62352GP-TFB MBM29F400TC-70PFTN NJM12903R-TFB NJM13403V-TFB NJM13404V-TFB		D 301,	D 702 D 302	KV1470 KV1870S LT1KS67A
				SWIT	CHES		
	IC121 IC100		NJM319V-TFB		S301 S601		DSG1065 DSG1071
	IC115		NJM3414AV-TFB PCM1719E	COIL	S AND	FILTERS	
Δ	IC602 IC900 IC109 IC405 IC311		PE5131A PE5214A PM0025AF PQ20WZ11 PST9243NR		L 902 L 904)-L 1002,L 1004,L 1007,L 100	LCYA2R7J2520 LCYA8R2J2520
	IC503 IC501 IC107 IC904 IC105	,	RL5E839 SM8706AV SN74AHC2G66HDCT SN74LV125APW TC4W53FU		L 105-	i,L 1006 -L 108 -F 404, F 406	LCYAR68J2520 PTL1014 QTF1025 VTL1079

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	L 503- L 109		VTL1080 VTL1084		C 520, C 521	C 806, C 823, C 842	CKSRYB473K16 CKSRYB562K50
CAPA	ACITOF	L 402, L 403, L 905–L 907	VTL1109			1,C 143, C 301, C 508, C 509 C 514, C 836	CKSRYF103Z50 CKSRYF103Z50
	C 720,	C 740, C 922 C 236, C 237, C 704	CCSRCH100D50 CCSRCH101J50 CCSRCH102J50		C 1006	5,C 101, C 103, C 104, C 110 2,C 1106,C 1108,C 111	
	C 147, C 231,	C 911 C 232, C 835	CCSRCH120J50 CCSRCH151J50		C 1112 C 1123 C 1132	2,C 1113,C 112, C 1121 3-C 1126,C 1128,C 113 2-C 1134,C 114–C 116	CKSRYF104Z25 CKSRYF104Z25 CKSRYF104Z25
	C 450 C 905 C 168,	C 169, C 172	CCSRCH181J50 CCSRCH220J50 CCSRCH221J50		•	C 119, C 122, C 126, C 127 C 132, C 133, C 136, C 139	
	C 239,	C 213 C 240	CCSRCH270J50 CCSRCH271J50		C 162, C 173-	C 149, C 152–C 157, C 160 C 163, C 165–C 167 -C 178, C 184, C 186, C 191	CKSRYF104Z25 CKSRYF104Z25
	C 205, C 243 C 235	C 920	CCSRCH330J50 CCSRCH331J50		•	C 197, C 203, C 204 C 209, C 230, C 233, C 238	CKSRYF104Z25 CKSRYF104Z25
	C 708, C 140	C 833	CCSRCH391J50 CCSRCH471J50 CCSRCH4R0C50		C 245, C 313- C 323,	C 246, C 302–C 311 -C 315, C 318–C 320 C 324, C 326, C 327, C 402	CKSRYF104Z25 CKSRYF104Z25 CKSRYF104Z25
	C 723 C 921	C 513	CCSRCH560J50 CCSRCH5R0C50 CCSRCH6R0D50		•	C 406, C 408, C 409, C 425 -C 507, C 515, C 516, C 519	
	C 1103 C 1129	3,C 1109,C 411 3,C 410, C 424 4,C 1115,C 1122,C 1127	CEV100M16 CEV101M16 CEV470M6R3		C 522, C 607- C 622,	C 524-C 532, C 602 -C 611, C 614, C 618, C 619 C 623, C 625, C 627, C 628 -C 809, C 811, C 812, C 816	CKSRYF104Z25 CKSRYF104Z25 CKSRYF104Z25
	C 107, C 706,	C 108, C 1105, C 1130, C 70 C 915	1 CKSQYB105K10 CKSQYB105K10		C 824,	C 831, C 90, C 901–C 904 C 912, C 916, C 924–C 926	CKSRYF104Z25 CKSRYF104Z25
	C 164,	C 423, C 426, C 917–C 919 C 170, C 312, C 317, C 501 C 604, C 606, C 612, C 613	CKSQYF225Z16		C 99 C 1119	9,C 138, C 146, C 629, C 631 C 703, C 707, C 711, C 713	CKSRYF104Z25 CKSRYF105Z10
	C 615,	C 616, C 620, C 621, C 624 C 630, C 804, C 810, C 839	CKSQYF225Z16		C 717,	C 721, C 722, C 731, C 733 5,C 1117	
	C 1002	2,C 106, C 1120,C 131, C 18	5 CKSRYB102K50		C 189, C 403,	C 190 (10μF/16V) C 405, C 407 (220μF/10V) 7,C 1138 (4.7μF/16V)	DCH1121 DCH1136 DCH1142
	C 718, C 832,	C 215, C 322, C 712, C 716 C 719, C 732, C 737, C 738 C 88, C 89, C 91, C 914	CKSRYB102K50 CKSRYB102K50		C 1104	4 (2.2μF/10V)	VCG1031
	C 92–0 C 109,	C 117, C 135, C 141, C 142	CKSRYB102K50 CKSRYB103K50			C 192 (4.7μF/6.3V) ,VC702 (20p)	VCG1039 VCM1008
		C 193, C 211, C 316, C 705 C 814, C 844, C 909, C 910		RESI	STORS	R 170	RAB4C0R0J
	C 123,	1,C 102, C 105, C 1135,C 11 C 124, C 128, C 130	CKSRYB104K16		R 626	R 150, R 316, R 317, R 332	RAB4C102J
		C 145, C 171, C 179–C 183 C 710, C 801–C 803, C 805				R 472, R 620, R 625 R 640	RAB4C103J RAB4C103J
	C 1110	C 845, C 906, C 907, C 913),C 1111 C 821, C 822, C 825, C 830	CKSRYB122K50			R 619, R 621, R 622 3,R 179, R 190, R 816, R 817	RAB4C220J RAB4C223J
	C 843		CKSRYB222K50		R 230,	R 815, R 822, R 823 R 452–R 455, R 511, R 512 R 634, R 635, R 638	RAB4C303J RAB4C330J RAB4C470J
		C 207, C 210, C 838, C 840 3,C 198	CKSRYB223K50 CKSRYB224K10 CKSRYB331K50		R 303	55 1, 11 555, 11 555	RAB4C560J
	C 201,	C 714, C 817–C 820 -C 829	CKSRYB332K50 CKSRYB332K50		R 1104	-R 805 4,R 819, R 821, R 824, R 825	
	C 715 C 923		CKSRYB333K16 CKSRYB392K50		R 244 R 839,	R 841	RS1/16S1100F RS1/16S1203F
		C 121, C 125, C 134, C 137 C 518	CKSRYB393K16 CKSRYB472K50 CKSRYB472K50		R 250 R 401,	R 402 R 248	RS1/16S1203F RS1/16S1500F RS1/16S2001F RS1/16S3302F RS1/16S3600F

DVR-A03

Mark	No. Description	Part No.
	R 247 R 1156 R 245, R 251 VR103, VR104 (4.7kΩ) VR105 (10kΩ)	RS1/16S5600F RS1/16S5601F RS1/16S6802F ACP1091 DCP1080
	Other Resistors	RS1/16S □□□ J
OTHE	RS	
	JA101 MINI JACK CN402 ZH CONNECTOR 2P CN408 D-OUT CONNECTOR(2P) CN101 53P CONNECTOR CN601 3P CONNECTOR	
	CN301 4P CONNECTOR CN401 LK CONNECTOR (4IN1/AT)	DKN1221 LK-44104H-S1D1Z-2
	CN803 16P CONNECTOR CN801,CN802 4P CONNECTOR	SFW16R-2ST VKN1490
	X501 CRYSTAL RESONATOR (36.864MHz)	DSS1125
\triangle	TH402 POLY SWITCH	DCX1035

6. ADJUSTMENT

Adjustment Items

Perform the adjustment of this model in the order as shown below.

Adjustment and confirmation of the main unit

6.2 Adjustment

Initial Setting

6.2.1 VCO Free-running Adjustment

[1st PLL Adjustment]

[2nd PLL Adjustment]

6.2.2 Power Adjustment

(1) DVD Power Adjustment

(1.1) Playback Power Adjustment

(1.2) Recording Power Adjustment

[Write Power Low Adjustment]

[Write Power High Adjustment]

[Erase Power APC Low Adjustment]

[Erase Power APC High Adjustment]

[RW Erase Power Low Adjustment]

[RW Erase Power High Adjustment]

(2) CD Power Adjustment

(2.1) Playback Power Adjustment

(2.2) Recording Power Adjustment

[Write Power Low Adjustment]

[Write Power High Adjustment]

[Erase Power Low Adjustment]

[Erase Power High Adjustment]

[Erase Power APC Low Adjustment]

[Erase Power APC High Adjustment]

[RW Erase Power Low Adjustment]

[RW Erase Power High Adjustment]

6.2.3 Radial Tilt Circuit Adjustment

6.2.4 Focus Position Adjustment

[DVD-ROM (Dual) Adjustment]

[Focus Position Adjustment of Layer 0]

[Focus Position Adjustment of Layer 1]

6.2.5 Wobble SPDL Bias Adjustment

6.2.6 Playback Ability Confirmation

6.2.7 Recording Ability Confirmation

Note:

When Traverse Mechanism Assy-S is replaced, adjustment of the mechanism section is not required because of it's adjusted already.

Measuring Instruments and Tools

Use disc

• DVD-ROM (Single) disc
• DVD-ROM (Dual) disc GGV1036
• New DVD-R disc GGV1049
• New DVD-RW disc
• CD-ROM and CD-DA disc GGV1054
• New CD-R disc GGX1011
• New CD-RW disc
• Recorded DVD-R disc(
• Recorded DVD-RW disc ()
• Recorded CD-R disc
• Recorded CD-RW disc

Measuring instruments

- Digital multimeter
- Oscilloscope (with monitor output)
- Light power meterTQ8210 or equivalent
- Jitter meter KJM6765S or equivalent

Control

- DOS-V Personal computer (for command transmission: RS-232C port)
- General-purpose communication software

Others

• Adjustment screwdriver

Adjustment Points and Their Names

VC701: 1st PLL adjustment VC702: 2nd PLL adjustment

VR103: DVD playback power adjustment VR104: CD playback power adjustment

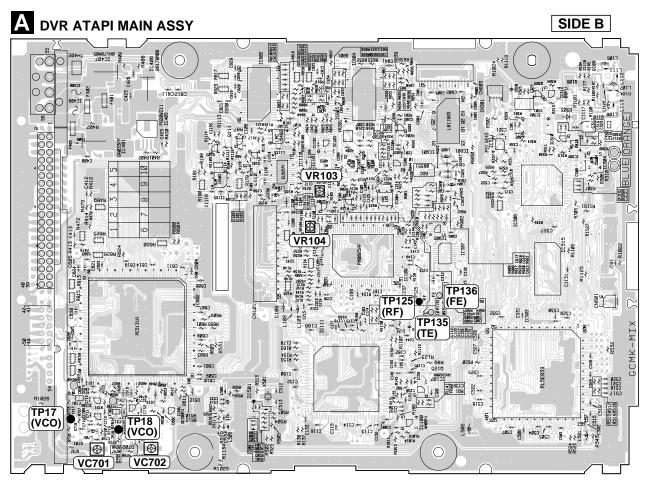


Fig.1 Adjustment point

NECESSARY ADJUSTMENT POINTS

When **Adjustment Points ■ EXCHANGE TRAVERSE MECHA ASSY** Mechanical Exchange point TRAVERSE MECHANISM ASSY-S Electric Adjustment and confirmation of the main unit point **■ EXCHANGE PCB ASSY** Mechanical Exchange board point **DVR ATAPI MAIN ASSY** Electric point Adjustment and confirmation of the main unit

6.1 TEST MODE

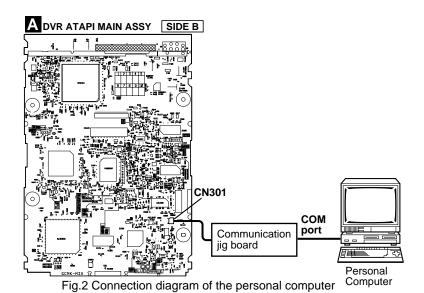
6.1.1 Sending Test Mode Commands

To operate this unit directly in Test mode, connect the COM port of the personal computer with CN301 in the DVD ATAPI MAIN Assy via interface.

To send commands, use RS-232C general-purpose communication software (e.g. WTERM, CCT). Communication protocols are as follows:

Baud rate : 38400 (fixed)

Character length : 8 bit
Stop bit : 1 bit
Parity : none
Flow control : none
Others : LSB 1st



6.1.2 Disc Selection

To set the 4.7GB DVR mode, enter the code "5DT" from the communication software.

This operation calls as "Selects 4.7R mode".

It becomes each disc mode when entering the following codes.

Enter code	Mode
"0DT"	: "Selects CD-ROM mode"
"1DT"	: "Selects CD-R mode"
"2DT"	: "Selects CD-RW mode"
"3DT"	: "Selects DVD-ROM (Single) mode"
"4DT"	: "Selects DVD-ROM (Dual) mode"
"7DT"	: "Selects DVD-RWmode"

6.2 ADJUSTMENT

Initial Setting

Short-circuit with jumper pin at the second (MA and SL) from the right side of the short-pin while looking from the rear side. (Test mode) Enter code "9AJ". (Taking in command of adjustment initial value.)

Note: This command does not need to issue it once again if issued it once. However, perform the Power Adjustment surely afterwards when issued this command.

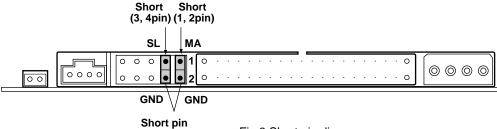


Fig.3 Short pin diagram

■ Adjustment and confirmation of the main unit Initial Setting

6.2.1 VCO Free-running Adjustment

	<u> </u>		
Objective			
Symptom when out of adjustment			
Measurement Instru- ment connections	Connect the digital multimeter to TP17 and TP18.	Player state	POWER ON
Adjustment standard	[1st PLL adjustment] 2.5V ± 0.01V	Adjustment location	VC701 and VC702
value	[2nd PLL adjustment] 2.5V ± 0.01V	Disc	None needed

[Procedure]

Enter the RS-232C command.

"6MS"

"+A4+AS"

"+0E+DW" (Enter the VCO free-running adjustment mode)

[1st PLL Adjustment]

Adjust VC701 so that the voltage of TP17 (periphery of IC602 R3 chip) becomes $2.5V \pm 0.01V$.

[2nd PLL Adjustment]

Adjust VC702 so that the voltage of TP18 becomes $2.5V \pm 0.01V$.

"+00+DW" (Release from the VCO free-running mode)

6.2.2 Power Adjustment

Before adjustment, turn VR103 and VR104 (periphery of CN101) fully counterclockwise to set their laser power output to minimum.

(1) DVD Power Adjustment

• Set the wavelength of the light power meter to 660 nm, and shine the sensor to the objective lens.

(1.1) Playback Power Adjustment

Objective	To optimize the playback power of laser diode (LD).			
Symptom when out of adjustment	When a gap is terrible : Player does not playback, track search is impossible When a gap is light : RF waveform is dirty.			
Measurement Instrument connections	Shine the light emitted from the objective lens on the light power meter sensor. Wavelength 660nm Ave. mode	Player state Adjustment location		
Adjustment standard value	Wavelength 660nm, 1.03 ± 0.03mW (Ave.)	Disc		

[Procedure]

"5DT" (Selects 4.7R mode)

"LD" (LD ON)

Adjust VR103 so that the indication of light power meter becomes 1.03 ± 0.03 mW.

"LD" (LD OFF)

Note: When confirm the output power once again after the Playback Power Adjustment, if indication of the light power meter is limit of 1.03 \pm 0.06mW, ther is not a problem.

(1.2) Recording Power Adjustment

1					
Objective	To optimize the playback power of laser diode (LD).				
Symptom when out of adjustment	When a gap is terrible : Player does not playback, track search is impossible When a gap is light : RF waveform is dirty.				
Measurement Instru-	Shine the light emitted from the objective lens on the light power meter sensor.	Player state	STOP		
Wavelength 660nm Ave. mode		Adjustment location	Set the value with the command		
		Disc	None needed		

[Procedure]

[Write Power Low Adjustment]

"1AW"

Adjust with UP/DN command so that the indication of light power meter becomes 5.4 ± 0.2 mW. (When enters the "5UP/5DN", it can send every 5 step.)

"EE" (Store the adjustment value in the nonvolatile memory)

Write Power High Adjustment]

"0AW"

Adjust with UP/DN command so that the indication of light power meter becomes 10.7 ± 0.2 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

Selects DVD-RW mode.

[Erase Power APC Low Adjustment]

"5AW"

Adjust with UP/DN command so that the indication of light power meter becomes 5.4 ± 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

[Erase Power APC High Adjustment]

"4AW"

Adjust with UP/DN command so that the indication of light power meter becomes 10.8 ± 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

[RW Erase Power Low Adjustment]

"7A\//"

Adjust with UP/DN command so that the indication of light power meter becomes 1.07 ± 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

[RW Erase Power High Adjustment]

"6AW"

Adjust with UP/DN command so that the indication of light power meter becomes 1.13 ± 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

(2) CD Power Adjustment

• Set the wavelength of the light power meter to 780 nm, and shine the sensor to the objective lens.

(2.1) Playback Power Adjustment

Objective	To optimize the playback power of laser diode (LD).			
Symptom when out of adjustment	When a gap is terrible : Player does not playback, track search is impossible When a gap is light : RF waveform is dirty.			
Measurement Instru-	Shine the light emitted from the objective lens on the light power meter sensor.	Player state	STOP	
	Wavelength 780nm Ave. mode	Adjustment location	VR104	
Adjustment standard value	Wavelength 780nm, 1.26 ± 0.03mW (Ave.)	Disc	None needed	

[Procedure]

"1DT" (Selects CD-R mode)

"LD" (LD ON)

Adjust VR104 so that the indication of light power meter becomes 1.26 \pm 0.03mW.

"LD" (LD FF)

Note: When confirm the output power once again after the Playback Power Adjustment, if indication of the light power meter is limit of 1.26 \pm 0.06mW, there is not a problem.

(2.2) Recording Power Adjustment

Objective	To optimize the playback power of laser diode (LD).			
Symptom when out of adjustment	When a gap is terrible : Player does not playback, track search is impossible When a gap is light : RF waveform is dirty.			
Measurement Instru-	Shine the light emitted from the objective lens on the light power meter sensor.	Player state	STOP	
	Wavelength 780nm Ave. mode	Adjustment location	Set the value with the command	
		Disc	None needed	

[Procedure]

[Write Power Low Adjustment]

"1AW"

Adjust with UP/DN command so that the indication of light power meter becomes $3.4 \pm 0.1 \text{mW}.$

"EE" (Store the adjustment value in the nonvolatile memory)

[Write Power High Adjustment]

"0AW"

Adjust with UP/DN command so that the indication of light power meter becomes $5.9 \pm 0.1 \text{mW}$.

"EE" (Store the adjustment value in the nonvolatile memory)

[Erase Power Low Adjustment]

"3AW"

Adjust with UP/DN command so that the indication of light power meter becomes 3.6 ± 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

[Erase Power High Adjustment]

"2AW"

Adjust with UP/DN command so that the indication of light power meter becomes 6.5 ± 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

[Erase Power APC Low Adjustment]

"2DT" (Selects CD-RW mode)

"5AW"

Adjust with UP/DN command so that the indication of light power meter becomes 7.6 ± 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

[Erase Power APC High Adjustment]

"4AW"

Adjust with UP/DN command so that the indication of light power meter becomes 15.1 \pm 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

[RW Erase Power Low Adjustment]

"7AW"

Adjust with UP/DN command so that the indication of light power meter becomes 5.3 ± 0.1 mW.

"EE" (Store the adjustment value in the nonvolatile memory)

[RW Erase Power High Adjustment]

"6AW"

Adjust with UP/DN command so that the indication of light power meter becomes $10.2 \pm 0.1 \text{mW}$.

"EE" (Store the adjustment value in the nonvolatile memory)

6.2.3 Radial Tilt Circuit Adjustment

Objective	To adjust the target value of tilt servo so that pickup and disc become to be level relatively.				
Symptom when out of adjustment	Playback RF waveform is dirty (Playback jitter is defective).				
Measurement Instru- ment connections	Connect the total T-jitter meter to TP125 (RF) terminal.	Player state	PLAY, Tilt servo ON		
		Adjustment location	Set the tilt error value with the command input.		
Adjustment standard value	Playback jitter is minimum.	Disc	DVD-ROM(Dual)/ DVD-ROM(Single)/ Unrecorded DVD-RW/ Recorded CD-R discs.		

[Procedure]

- "3TL" (Initialize the tilt)
- Enters code "4TL" in the state that does not clamp a disc.
- Calmp the unrecorded DVD-RW disc and enters code "5TL".
- Calmp the DVD-ROM (Dual) disc and enters code "6TL".
- Calmp the DVD-ROM (Single) disc.
 - "3DT" (Selects DVD-ROM (Single) mode)
 - "1XN" (Set the CLV normal speed)
 - "+100000+PL" (Search for address 100000h)
- Monitor the pin 54 (AGCOUT) of IC112 (RF63). ("RF" is marked on the test land of the DVD ATAPI MAIN Assy.)
- Connect the jitter meter to TP125 (RF), search for a point where the jitter of both total-T edges become minimum with "1TL" (Tilt UP) / "2TL" (Tilt Down). At this time, turn the equalizer of jitter meter to OFF.
 - "7TL" (Obtain the TILT TARGET)
 - "RJ" (REJECT)
- Clamp the recorded CD-R disc.
 - "1DT" (Selects CD-R mode)
 - "4XN" (Set the CLV 4th speed)
 - "+200000+PL" (Search for 20 minutes)
- Monitor the pin 54 (AGCOUT) of IC112 (RF63). ("RF" is marked on the test land of the DVD ATAPI MAIN Assy.)
- Connect the jitter meter to TP125 (RF), search for a point where the jitter of both total-T edges become minimum with "1TL" (Tilt UP) / "2TL" (Tilt Down). At this time, turn the equalizer of jitter meter to OFF.
- "7TL" (Obtain the TILT TARGET)
- "RJ" (REJECT)

6.2.4 Focus Position Adjustment

Objective	To optimize the playback characteristic of the RF signal.		
Symptom when out of adjustment	Playback RF waveform is dirty (Playback jitter is defective). REC/PLAY RF waveform is dirty (REC/PLAY jitter is defective).		
Measurement Instru- ment connections	Connect the total T-jitter meter to TP125 (RF) terminal.	Player state Adjustment location	PLAY, tilt servo ON Set the DAC value with the command input.
Adjustment standard value	Playback jitter is minimum.	Disc	DVD-ROM (Single)/ DVD-ROM (Dual)/ Recorded CD-R/ New DVD-RW discs.

[Procedure]

• Clamp the DVD-ROM (Single) disc.

"3DT" (Selects DVD-ROM (Single) mode)

"#+99070000+FR" (ACT sensitivity adjustment)

Note: Issue the CD-ROM disc only.

"1XN" (Set the CLV normal speed)
"+100000+PL" (Search for address 100000h)

"0MS"

• Connect the jitter meter to TP125 (RF) and adjust "+****+DW" command so that the jitter of the both total-T edges become minimum, and focus position will be changed. (Value to input into **** performs coarse adjustment with 0400h step and fine adjustment with 0100h step.)

"FE" (Store the adjustment value in the nonvolatile memory)

"RJ" (REJECT)
"RS" (RESET)

• Perform the Focus Position Adjustment as same step as in the recorded DVD-R and DVD-RW discs.

[DVD-ROM (Dual) Adjustment]

Adjust the layer 0 and layer 1 of DVD-ROM (Dual) disc together.

[Focus Position Adjustment of layer 0]

"4DT" (DVD-ROM Dual mode)
"1XN" (Set the CLV normal speed)
"+100000+PL" (Search for address 100000h)

"0MS" "0AS"

"EE" (Store the adjustment value in the nonvolatile memory)

[Focus Position Adjustment of layer 1]

"2FC" (Focus Jump UP (layer 0 to layer 1))

"0MS" "0AS"

"EE" (Store the adjustment value in the nonvolatile memory)

CD System Adjustment

Boot the CD system disc.

"+99070000+FR" (ACT sensitivity adjustment)

Note: Issue the disc only.

"4XN" (Set the CLV 4th speed)

"PL" (PLAY)

"+2000000+FR" (TOC information readout, etc.)
"+200000+PL" (Search for 20 minutes)

• Perform the Focus Position Adjustment as same step in the recorded CD-R and CD-RW discs.

6.2.5 Wobble SPDL Bias Adjustment

Objective	Correct the dispersion of spindle motor.			
Symptom when out of adjustment	Recording performance becomes poor, and jitter value of self recording/playback becomes outside of standard specification.			
Measurement Instru- ment connections	Player state PLAY			
ment connections	Adjustment location None			
		New 4.7GB DVD-R disc		
[Procedure]				
Clamp the unrecorded 4.7GB DVD-R disc. "PL" (PLAY) "+99050000+FR" (Wobble SPDL adjustment command) "2XN" (Set the CLV double speed) "+99050000+FR" (Wobble SPDL adjustment command) "RJ" (REJECT) "RS" (RESET)				

6.2.6 Playback Ability Confirmation

Symptom when out of adjustment	Confirm that the adjustment was done correctly.		
Measurement Instru- ment connections	Connect the total T-jitter meter to TP125 (RF) terminal.	Player state	PLAY
Adjustment standard value	jitter is less than 12%.	Adjustment location Disc	None Recorded DVD-R disc Recorded CD-R disc

[Procedure]

(1) DVD System

• Clamp the recorded DVD-R disc.

"5DT" (Selects 4.7R mode)

"1XN" (Set the CLV normal speed)

"PL" (PLAY)

Connect the jitter meter to TP125 (RF) and measure the jitter of both total-T edges. Confirm that jitter is less than 12%.

"RJ" (REJECT)
"RS" (RESET)

(2) CD System

• Clamp the recorded CD-R disc.

"1DT" (Selects CD-R mode)

"4XN" (Set the CLV 4th speed)

"PL" (PLAY)

"+20000000+FR" (TOC information readout, etc.)

Connect the jitter meter to TP125 (RF) and measure the jitter of both total-T edges. Confirm that jitter is less than 12%.

"RJ" (REJECT)
"RS" (RESET)

6.2.7 Recording Ability Confirmation

Symptom when out of adjustment Confirm that the adjustment was done correctly.				
Measurement Instru- ment connections		Player state	PLAY	
Adjustment standard value	jitter is less than 12%.	Adjustment location Disc	None New DVD-R disc New CD-R disc	
[Procedure]				
(1) DVD System				
Clamp the New DVD-R dis	SC.			
"5DT" (Selects 4.7R m				
,	LV normal speed)			
"PL" (PLAY)	-1 -2 -7			
"+20000000+FR"	(LPP information readout,	etc.)		
"OE" (OPC END		,		
Address of result of OPC	END SEEK calls as "*****h".			
Following OW and OR c	ommands enter the address which	n subtructed 1 from the above addre	ess.	
"+****+OW"	(Perform OPC from the addre	ess *****h)		
"+****+OR"	,			
"+E00+LN"				
"+****+WR"	(Test write. *****h is start a	address and set the physical ad	ldress.)	
"RJ"	(REJECT)	. ,	,	
"+****+PL"	(Measure the self recording/p	playback jitter and confirm that j	itter is less than 12%.)	
"RJ"	(REJECT)		,	
"RS"	(RESET)			
(2) CD System				
Clamp the New CD-R disc				
"1DT" (Selects CD-R r				
,	LV 4th speed)			
"PL" (PLAY)	• ,			
"+20000000+FR"	(TOC information readout,	etc.)		
"OE" (OPC END	•	•		
Address of result of OPC	CEND SEEK calls as "*****h" (M	MSF). Meaning of MSF is minute, se	econd and frame.	
		n subtructed 5 from the above addre		
"5LN"	(Perform OPC of 5 frames)			
"+****+OW"	(Perform OPC from the addre	ess *****h)		
"+****+OR"	Outputs the OPC result from	•		
"+F00+LN"	(Test write the F00h frame)	·		
"+****+WR"	(Test write. *****h is start a	address and set the MSF.)		
"D !"	(DE IEOT)	·		

6.3 Release the Test mode

"RJ"

"RJ2"

"+****+PL"

Remove the short-pin which short-circuited in the initial setting, and release the Test mode.

(REJECT)

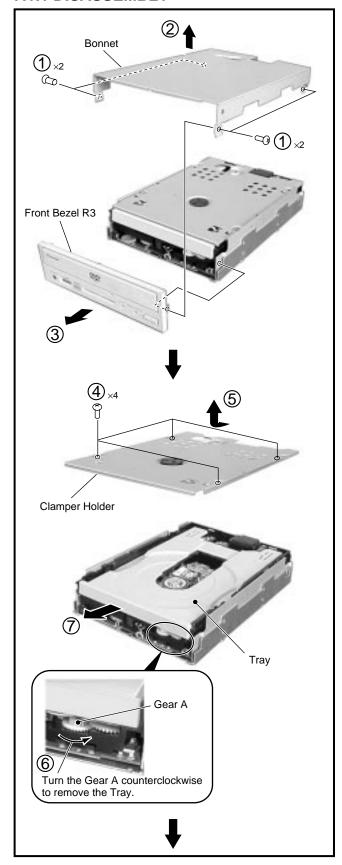
(REJECT)

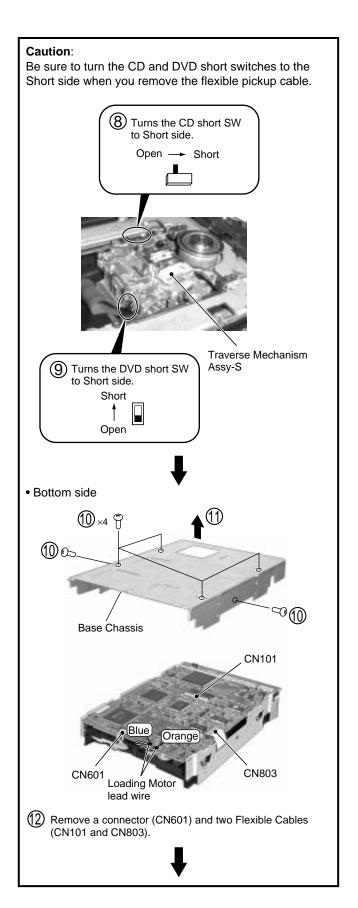
(Measure the self recording/playback jitter and confirm that jitter is less than 12%.)

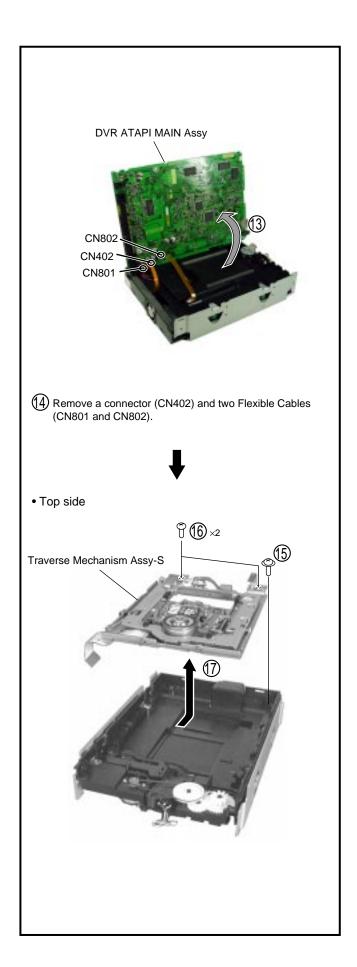
7. GENERAL INFORMATION

7.1 DIAGNOSIS

7.1.1 DISASSEMBLY

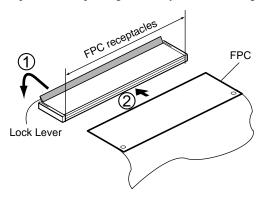






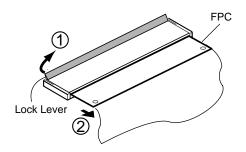
■ Connecting the Flexible Pickup Cable

- 1. Insert the FPC with the conductor side upward. Properly insert it to the slot until it stops.
- Push down both sides of the Lock Lever until they stop.
 It cannot be locked with one side only.
 Imperfection of pushing down may cause unlocking.



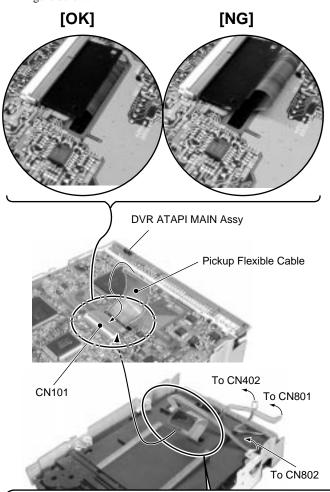
Disconnecting the flexible pickup cable

- 1. Pull up the Lock Lever upward.
- 2. After unlocking, pull out the FPC.



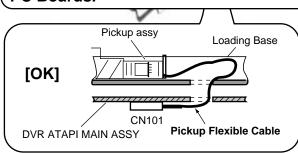
Styling the Flexible Cables

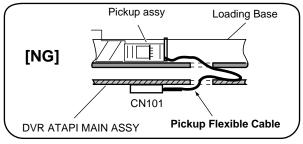
Perform styling of the Flexible Cables as shown in the figure below.



Cautions:

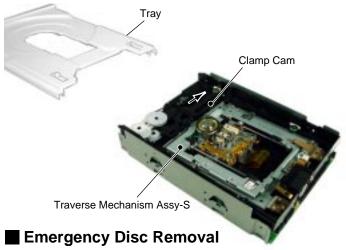
Be careful so that the Pickup flexible cable is not caught between the Loading base and PC Boards.





■ Caution When Installing the Tray

Confirm the position of Clamp Cam there is in the arrow direction.



In the following cases, discs can be ejected using the emergency ejection hole.

- Trouble with the device makes it impossible to remove the disc using the OPEN/CLOSE button or a software command.
- A disc that you need to eject remains inside the device but the power is off.
- Confirm that the power for the device is OFF and that the disc has stopped spinning.
- 2. Insert the accompanying pin for emergency ejection straight into the emergency ejection hole and press firmly.



3. Pull it out as far as you need to and remove the disc. (The disc tray will open about 5 to 10 mm.)

Notes:

- Make sure to use only the accompanying pin for emergency ejection. (No other object should be inserted.)
- Never attempt to forcibly eject a disc that is still rotating, as doing so could result in injury personal or in damage to the disc.
- Do not place items within 12 cm of the front of this device, as doing so could obstruct the disc ejection operation.

7.2 PARTS

7.2.1 IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

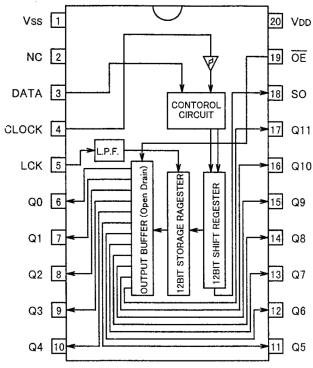
•List of IC

BU2099FV, BA5983FM, HY628100BLT1-70, AK6416AM, M11B416256A, SM8706AV, MBM29F400TC-70PFTN, UPC2511GK-9EU-X, UPD72153GM-UEU, PST9243NR, PM0025AF, M37902FGCHP

■ BU2099FV (DVR ATAPI MAIN ASSY : IC308)

• Serial In/Parallel Out Expander

Block Diagram



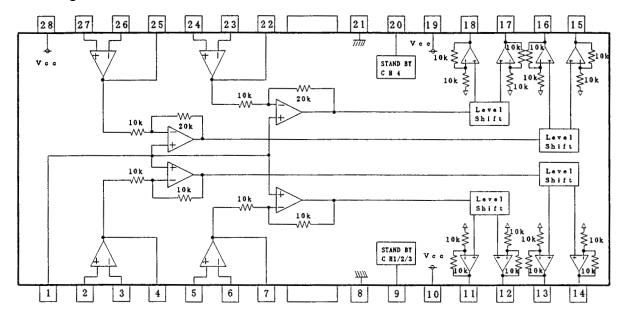
Pin Function

No.	Symbol	1/0	Function		
1	Vss	_	GND		
2	NC	-	Non Connection		
3	DATA		Input Serial Data		
4	CLOCK	1	Shift Clock (Rising Edge Trigger)		
5	LCK	1	Latch Clock (Rising Edge Trigger)		
6~17	Q0~Q11 (Qx)	0	O Output Parallel data(Nch Open Drain FET)		
			LATCH DATA L H		
			OUTPUT FET ON OFF		
18	so	0	Serial Output Data		
19	OE	1	Output Enable Control		
20	VDD		Power Supply		

^{*} OE Pull down to Vss

■ BA5983FM (DVR ATAPI MAIN ASSY : IC804)

- 4ch BTL Driver IC
- Block Diagram



resistor unit : Ω

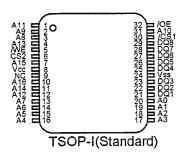
Pin Function

NO	Symbol	Function	NO	Symbol	Function
1	BIAS IN	Input for Bias—amplifier	15	VO4(+)	Non inverted output of CH4
2	OPIN1(+)	Non inverting input for CH1 OP-AMP	16	VO4(-)	Inverted output of CH4
3	OPIN1(-)	Inverting input for CH1 OP-AMP	17	VO3(+)	Non inverted output of CH3
4	OPOUT1	Output for CH1 OP-AMP	18	VO3(-)	Inverted output of CH3
5	OPIN2(+)	Non inverting input for CH2 OP-AMP	19	PowVcc2	Vcc for CH3/4 power block
6	OPIN2(-)	Inverting input for CH2 OP-AMP	20	STBY2	Input for CH4 stand by control
7	OPOUT2	output for CH2 OP-AMP	21	GND	Substrate ground
8	GND	Substrate ground	22	OPOUT3	Output for CH3 OP-AMP
9	STBY1	Input for CH1/2/3 stand by control	23	OPIN3(-)	Inverting input for CH3 OP-AMP
10	PowVcc1	Vcc for CH1/2 power block	24	OPIN3(+)	Non inverting input for CH3 OP-AMP
11	VO2(-)	Inverted output of CH2	25	OPOUT4	Output for CH4 OP-AMP
12	VO2(+)	Non inverted output of CH2	26	OPIN4(-)	Inverting input for CH4 OP-AMP
13	VO1(-)	Inverted output of CH1	27	OPIN4(+)	Non inverting input for CH4 OP-AMP
14	VO1(+)	Non inverted output of CH1	28	PreVcc	Vcc for pre block

notes) Symbol of + and - (output of drivers) means polarity to input pin. (For example if voltage of pin4 high,pin14 is high.)

■ HY628100BLT1-70 (DVR ATAPI MAIN ASSY : IC351)

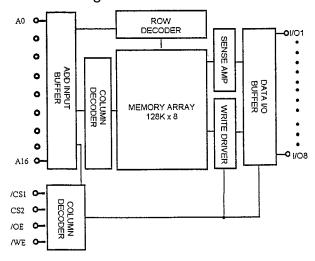
- SRAM (1Mbit)
- Pin Arrangement (Top view)



Pin Function

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
₩E	Write Enable
/OE	Output Enable
A0 ~ A16	Address Input
1/01 ~ 1/08	Data Input/Output
Vcc	Power(5.0V)
Vss	Ground

Block Diagram



AK6416AM (DVR ATAPI MAIN ASSY : IC309)

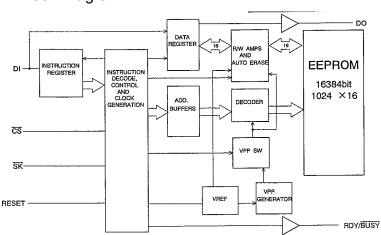
- EEPROM
- Pin Arrangement (Top view)



Pin Function

PIN NO.	DESCRIPTION	
CS	Chip select	
SK	Serial clock Input	
DI	Serial data Input	
DO	Serial data output	
RESET	Reset Input	
RDY/BUSY	RDY/BUSY output	
Vcc	Power supply	
GND	Ground	

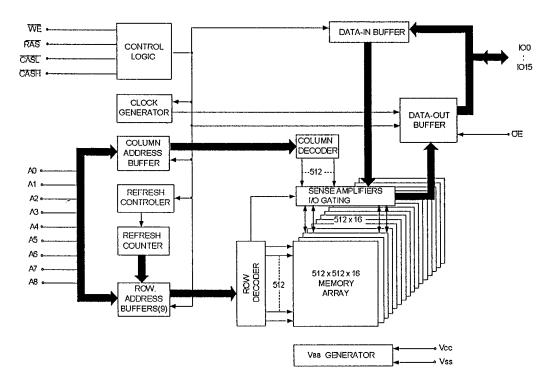
Block Diagram



■ M11B416256A-35T (DVR ATAPI MAIN ASSY : IC104)

• EDO RAM (4Mbit)

Block Diagram



Pin Function

PIN NO.	PIN NAME	TYPE	DESCRIPTION
16~19,22~26	A0~A8	Input	Address Input Row Address : A0~A8 Column Address : A0~A8
14	RAS	Input	Row Address Strobe
28	CASH	Input	Column Address Strobe / Upper Byte Control
29	CASL	Input	Column Address Strobe / Lower Byte Control
13	WE	Input	Write Enable
27	ŌĒ	Input	Output Enable
2~5,7~10,31~34,36~39	1/00 ~ 1/015	Input / Output	Data Input / Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

■ SM8706AV (DVR ATAPI MAIN ASSY : IC501)

• Clock Generator

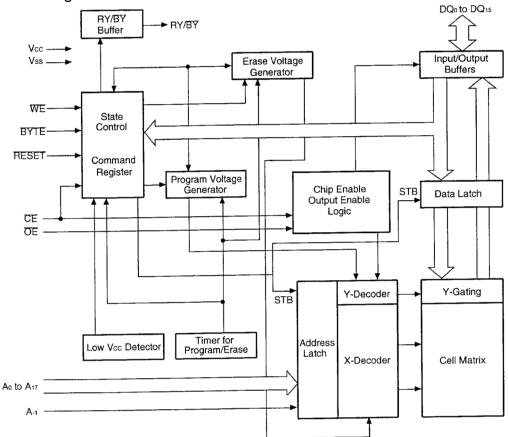
Block Diagram FSEL .**≢** AO1 Ref. Phase Charge LPF 0 VCO 0 Div. 0 ${\bf Detector 0}$ Pump0 XTI X'tal AO2 OSC XTO Loop Div. 0 (PLL0) - SO1 Control Logic Charge Ref. Phase LPF 1 VCO 1 Pump 1 Div. 1 Detector1 **■**SO2 Loop Div. 1 (PLL1) . MO2 \mathbf{CE}

Pin Function

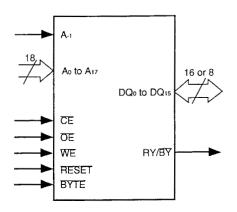
Number	Name	1/0	Function
1	VDD1	PWR	Supply 1 (for digital block)
2	VSS1	GND	Ground 1 (for digital block)
3	MO1	0	Video system output 1 (27MHz fixed)
4	MO2	0	Video system output 2 (54MHz fixed)
5	VDD2	PWR	Supply 2 (for analog block)
6	VSS2	GND	Ground 2 (for analog block)
7	XΤΙ	ı	Crystal oscillator connection or external clock input
8	хто	0	Crystal oscillator connection
9	A01	0	Audio system output 1 (384fs output)
10	A02	0	Audio system output 2 (768fs output)
11	VSS3	GND	Ground 3 (for digital block)
12	VDD3	PWR	Supply 3 (for digital block)
13	SO1	0	Signal processor system output 1 (16.9344MHz fixed)
14	FSEL	1	Sampling frequency select FSEL="H": fs=48kHz FSEL="L": fs=44.1kHz (with internal pull-up resistor, Schmitt-trigger input)
15	S02	0	Signal processor system output 2 (33.8688MHz fixed)
16	CE	ı	Chip enable ("H"=Enable, "L"=Disable)

■ MBM29F400TC-70PFTN (DVR ATAPI MAIN ASSY : IC313)

- Flash Memory (4Mbit)
 - Block Diagram



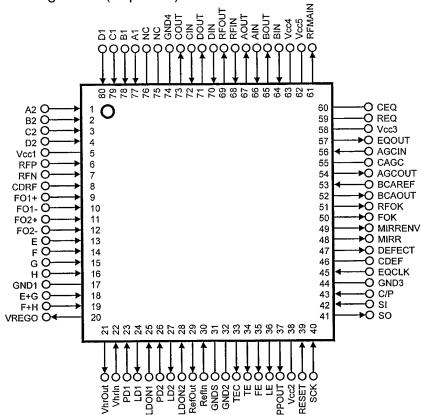
Pin Function

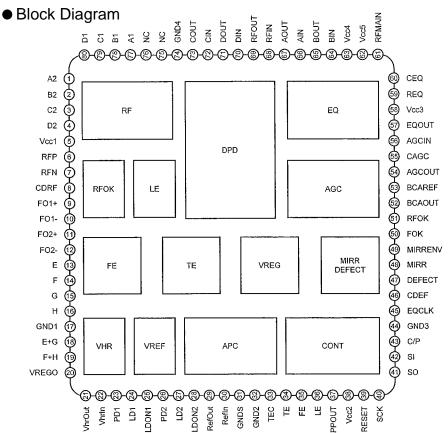


Pin	Function
A-1, A0 to A17	Address Inputs
DQ0 to DQ15	Data Inputs/Outputs
CE	Chip Enable
ŌE	Output Enable
WE	Write Enable
RY/BY	Ready-Busy Output
RESET	Hardware Reset Pin/ Temporary Sector Unprotection
BYTE	Selects 8-bit or 16-bit mode
N.C.	No Internal Connection
Vss	Device Ground
Vcc	Device Power Supply

■ UPC2511GK-9EU-X (DVR ATAPI MAIN ASSY : IC112)

- CD/DVD RF FEP
- Pin Arrangement (Top view)





● Pin Function (1/2)

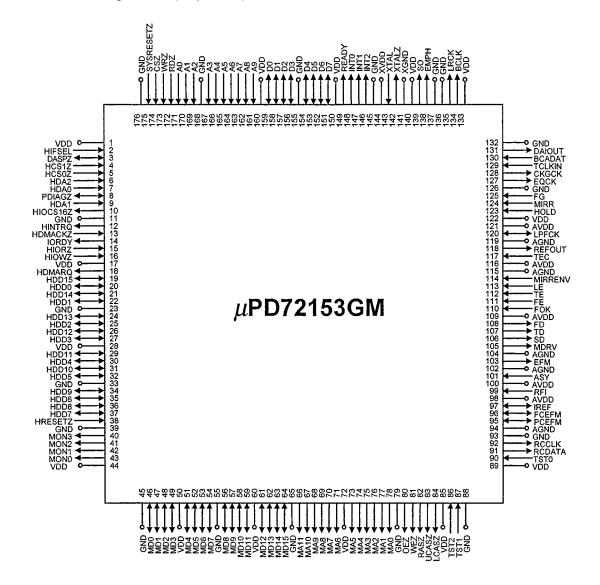
No.	Pin Name	Function	Input/Output
1	A2	A2 signal input	Input
2	B2	B2 signal input	Input
3	C2	C2 signal input	Input
4	D2	D2 signal input	Input
5	Vcc1	Power supply (5 V) pin	-
6	RFP	RF (differential signal) + input	Input
7	RFN	RF (differential signal) - input	Input
8	CDRF	RF signal input	Input
9	FO1+	FOCUS1+ signal input	Input
10	FO1-	FOCUS1- signal input	Input
11	FO2+	FOCUS2+ signal input	Input
12	FO2-	FOCUS2- signal input	Input
13	E	E signal input	Input
14	F	F signal input	Input
15	G	G signal input	Input
16	Н	H signal input	Input
17	GND1	GND	-
18	E+G	E+G signal input	Input
19	F+H	F+H signal input	Input
20	VREGO	Power output for monitor diode	Output
21	VhrOut	PDIC reference voltage output	Output
22	Vhrln	PDIC reference voltage input	Input
23	PD1	APC circuit 1 input	Input
24	LD1	APC circuit 1 output	Output
25	LDON1	APC circuit 1 laser on/off control	Input
26	PD2	APC circuit 2 input	Input
27	LD2	APC circuit 2 output	Output
28	LDON2	APC circuit 2 laser on/off control	Input
29	RefOut	Reference voltage output	Output
30	Refin	Reference voltage input	Input
31	GNDS	GND	-
32	GND2	GND	-
33	TEC	Track count signal output	Output
34	TE	Tacking error signal output	Output
35	FE	Focus error signal output	Output
36	LE	Lenz error signal output	Output
37	PPOUT	Push/pull signal output	Output
38	Vcc2	Power supply (5 V) pin	•
39	RESET	reset input	Input
40	SCK	Serial port clock input	Input

● Pin Function (2/2)

No.	Pin Name	Function	Input/Output
41	so	Serial data output	Output
42	SI	Serial data input	Input
43	C/P	Command (address)/parameter (data) identification signal input	Input
44	GND3	GND	_
45	EQCLK	Reference clock input for equalizer fc automatic adjustment circuit	Input
46	CDEF	Capacitor connection for bottom detection for defect detection circuit	-
47	DEFECT	Defect detection signal output	Output
48	MIRR	Mirror detection signal output	Output
49	MIRRENV	RF signal bottom envelop output for mirror comparator level setting	Output
50	FOK	RF peak envelop output for focus search	Output
51	RFOK	RF signal presence/absence judgment signal output	Output
52	BCAOUT	BCA circuit output	Output
53	BCAREF	BCA circuit comparator voltage input	Input
54	AGCOUT	AGC output	Output
55	CAGC	AGC charge pump capacitor connection	-
56	AGCIN	AGC amplifier input	Input
57	EQOUT	RF equalizer output	Output
58	Vcc3	Power source (5 V) pin	-
59	REQ	Resistor connection for equalizer current setting	-
60	CEQ	Capacitor connection for equalizer fc automatic adjustment circuit	-
61	RFMAIN	RF signal output (for monitoring)	Output
62	Vcc5	Power supply (5 V) pin	-
63	Vcc4	Power supply (5 V) pin	-
64	BIN	DPD B signal AC input	Input
65	BOUT	DPD B signal output (connect to BIN)	Output
66	AiN	DPD A signal AC input	Input
67	AOUT	DPD A signal output (connect to AIN)	Output
68	RFIN	DPD RF signal AC input	Input
69	RFOUT	DPD RF signal output (connect to RFIN)	Output
70	DIN	DPD D signal AC input	Input
71	DOUT	DPD D signal output (connect to DIN)	Output
72	CIN	DPD C signal AC input	Input
73	COUT	DPD C signal output (connect to CIN)	Output
74	GND4	GND	-
75	NC	Non Connection	-
76	NC	Non Connection	-
77	A1	A1 signal input	Input
78	B1	B1 signal input	Input
79	C1	C1 signal input	Input
80	D1	D1 signal input	Input

■ UPD72153GM-UEU (DVR ATAPI MAIN ASSY : IC111)

- 1-chip Controller
- Pin Arrangement (Top view)



Pin Function

Pins whose names have a bar above them (XXXX) are active low. Other pins are active high.

Note that the initial value indicates the status of the output pin at the time of reset. For the input pin, input the value specified at the time of reset.

<1> System interface

No.	Pin Name	Pin Function Description	1/0	Initial Value	Remarks
146, 147 148	INT2-INT0	μPD72153 interrupt request signals INT2: Servo interface-related interrupt request output INT1: Host interface-related interrupt request output INT0: Interrupt request output other than Servo and Host interface	0		5V_tolerant pins (others)
149	READY	Wait signal output to the local CPU during buffer memory access	0		5V_tolerant pin (others)
173	WR	Write control signal from the local CPU	1		5V_tolerant pin (others)
172	RD	Read control signal from the local CPU			5V_tolerant pin (others)
174	CS.	Chip select signal from the local CPU to the internal register and buffer memory	1		5V_tolerant pin (others)
161, 162 163, 164 165, 166 167, 169 170, 171	A9-A0	Address input signals. A9 is the MSB, and A0 is the LSB.			5V_tolerant pins (others)
151, 152 153, 154 156, 157 158, 159	D7-D0	Data input signals. D7 is the MSB, and D0 is the LSB	1		5V_tolerant pins (others)

<2> ATAPI interface (referred to SCSI controller DMA and MPEG decoder DMA interface)

No.	Pin Name	Pin Function Description	I/O	Initial Value	Remarks
14	IORDY	I/O channel ready signal to the host. It indicates that the drive is ready to receive transferred data. It is pulled up at 1.0 $k\Omega$ on the host side.	0		5V_tolerant pin (IDE)
15	DIOR	Read control signal from the host (HIFSEL pin = low)	1		Note 7
<u> </u> 		Read signal output when DMA transfer operation is performed for an external SCSI controller (HIFSEL pin = Hi)	0		5V_tolerant pin (IDE)
16	DIOM	Write control signal from the host (HIFSEL pin = low)	1		Note 7
		Write signal output when DMA transfer operation is performed for an external SCSI controller (HIFSEL pin = Hi)	0		5V_tolerant pin (IDE)

No.	Pin Name	Pin Function Description	1/0	Initial Value	Remarks
18	HDMARQ	DMA request signal output to the host (tristate) (HIFSEL pin = low)	0		5V_tolerant pin (IDE)
		Operates as a DREQ signal input pin when DMA transfer operation is performed for an external SCSI controller (HIFSEL pin = Hi)			
19, 21 24, 26	HDD15- HDD0	IDE data bus signal input/output pins (HIFSEL pin = low)	1/0		5V_tolerant pins (IDE)
29, 31 34, 36 37, 35 32, 30 27, 25 22, 20		16-bit data signal input/output pin used when data transfer operation is performed for an external SCSI controller (HIFSEL pin = Hi)	1/0		
38	HRESET	Reset signal input from the host	1		5V_tolerant pin (IDE)
2	HIFSEL	Signal used to select the host interface L: IDE interface; H: General-purpose DMA interface	!		5V_tolerant pin (IDE)
3	DASP	Pin used to input and output the device active and device 1 present signals for the IDE control bus. Pull up at 10 k Ω .	I/O		5V_tolerant pin (IDE)
4	HCS1	Control block register selection signal for the task register file	-		5V_tolerant pin (IDE)
5	HCS0	Command block register selection signal for the task register file			5V_tolerant pin (IDE)
6, 9, 7	HDA2- HDA0	IDE address bus input signals	I		5V_tolerant pins (IDE)
8	PDIAG	Pin used to input and output the password diagnostics signal for the IDE control bus. Pull up at 10 k Ω .	1/0		5V_tolerant pin (IDE)
10	HIOCS16	16-bit I/O output signal to the host. It indicates that 16-bit data can be transferred in the PIO transfer mode. Open drain output.	0		5V_tolerant pin (IDE)
12	HINTRQ	Interrupt request signal to the host	0		5V_tolerant pin (IDE)
13	HDMACK	DMA acknowledgement signal from the host. It indicates that the DMA transfer request has been accepted. (HIFSEL pin = low)	ı		5V_tolerant pin (IDE)
		Outputs the DACK signal when DMA transfer is performed for an external SCSI controller (HIFSEL pin = Hi)	0		

Note 7. Pull up at 10 K Ω .

<3> Buffer interface

No.	Pin Name	Pin Function Description	1/0	Initial Value	Remarks
64, 63 62, 61 59, 58 57, 56 54, 53 52, 51 49, 48 47, 46	MD15- MD0	16-bit data input/output pins for the buffer memory	I/O		5V_tolerant pins (others)
66, 67 68, 69 70, 71 73, 74 75, 76 77, 78	MA11- MA0	Address output pins for the buffer memory	0		3V pins
80	OE.	Output pin connected to the DRAM OE signal	0		3V pin
81	WE	Output pin connected to the DRAM WE signal	0		3V pin
82	RAS	RAS signal output pin	0		3V pin
83	UCAS	UCAS signal output pin	0		3V pin
84	LCAS	TCAS signal output pin	0		3V pin

<4> BCA channel interface

No.	Pin Name	Pin Function Description	I/O	Initial Value	Remarks
130	BCADAT	BCA signal input pin	1		3V pin

<5> Audio interface

No.	Pin Name	Pin Function Description	1/0	Initial Value	Remarks
134	BCLK	Synchronization clock output pin for serial voice data. Serial data changes at the falling edge of this clock.	0		3V pin
135	LRCK	Signal used to distinguish between S0 serial voice data L and R	0		3V pin
139	so	Serial voice data output pin. Data is output MSB first as a 2's complement and justified to LSB, in response to the change point of LRCK.	0		3V pin
138	EMPH	Emphasis identification signal	0		3V pin
131	DAIOUT	Digital audio output pin	0		3V pin

<6> Servo interface

No.	Pin Name	Pin Function Description	1/0	Initial Value	Remarks
105	MDRV	Spindle drive output pin	0	Undefined	Analog pin ^{Note 8}
106	SD	Thread drive output pin	0	Undefined	Analog pin ^{Note 8}
107	TD	Tracking drive output pin	0	Undefined	Analog pin ^{Note 8}
108	FD	Focus drive output pin	0	Undefined	Analog pin ^{Note 8}
123	HOLD	HOLD control signal input pin	ı		5V_tolerant pin (others)
124	MIRR	MIRR detection signal input pin	1		5V_tolerant pin (others)
110	FOK	RF signal peak envelop waveform input for focus search	-		Analog pin
114	MIRRENV	RF signal bottom envelop waveform input for MIRR signal comparator level setting	1		Analog pin
111	FE	Focus error signal input pin	1		Analog pin
112	TE	Tracking error signal input pin	ı		Analog pin
113	LE	Lenz error signal input pin	1		Analog pin
117	TEC	Tracking comparator input pin. Input a tracking error signal with the DC component cut. This signal detects tracking zero cross.	1		Analog pin
118	REFOUT	A/D converter mid-point potential output pin It can be used as a reference potential for the RF amplifier.	0	1/2VDD	Analog pin
125	FG	FG signal input pin	ı		5V_tolerant pin (others)

Note 8. The electric potential is undefined during the reset. It is fixed to 1/2VDD about 60 μ sec (maximum) after the power is turned on or the reset is canceled (XTAL must be oscillating). To protect the mechanical part, keep the driver powered off until the device is activated.

<7> Read channel interface

No.	Pin Name	Pin Function Description	1/0	Initial Value	Remarks		
92	RCCLK	Bit clock monitor pin	0		3V pin		
91	RCDATA	NRZI data monitor pin used after bit clock synchronization CD: EFM DVD: (8.16) is output.	3V pin				
127	EQCK	RF amplifier programmable equalizer reference clock output	3V pin				
128	CKGCK	Clock generator clock monitor pin		3V pin			
99	RFI	EFM comparator RF signal input pin					
101	ASY	EFM comparator level input	1		Analog pin		
103	EFM	EFM signal output pin O Analo					
95	PCEFM	Pull down to AGND using the 4700-pF capacitor.					
96	FCEFM	Pull down to AGND using the 1-μF capacitor. I/O Analog					
97	IREF	PLL reference current input pin	1		Analog pin		

<8> Monitor information

No.	Pin Name	Pin Function Description	1/0	Initial Value	Remarks
43	MON0	Outputs test signals.	0		3V pin
42	MON1	Outputs test signals.	0		3V pin
41	MON2	Outputs test signals.	0		3V pin
40	MON3	Outputs test signals.	0		3V pin

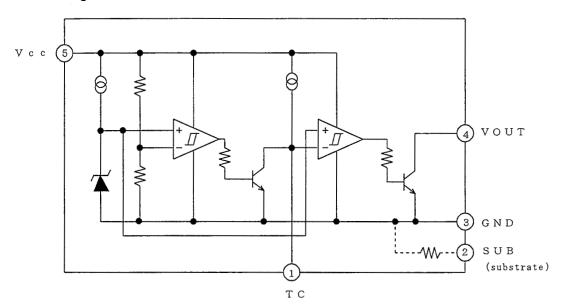
<9> Other signals

No.	Pin Name	Pin Function Description	1/0	Initial Value	Remarks
175	SYSRST	μPD72153 reset input pin	I		5V_tolerant pin (others)
142	XTAL	Crystal oscillator connection pin	0		
143	XTAL	Crystal oscillator connection pin	ı		
144	XVDD	Positive power source pin of the crystal oscillator	ı		
141	XGND	GND pin of the crystal oscillator			
121, 116 109, 100 98	AVDD	Analog positive power source pins			
119, 115 104, 102 94	AGND	Analog GND pins	1		
1, 17, 28 44, 50 60, 72 85, 89 122, 133 140, 150 160	VDD	Digital positive power source pins	1		
11, 23 33, 39 45, 55 65, 79 88, 93 126, 132 136, 137 145, 155 168, 176	GND	Digital GND pins	1		
129	TCLKIN	Test pin (Be sure to connect it to GND.)	1	-	3V pin
120	LPFCK	Test pin (Be sure to connect it to GND.)	1/0		Analog pin
86, 87 90	TST2-0	Test pins (Be sure to connect them to GND.)	1		3V pins

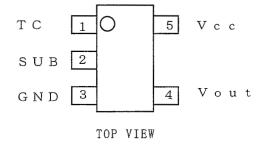
■ PST9243NR (DVR ATAPI MAIN ASSY : IC311)

• Reset IC

Block Diagram



Pin Arrangement (Top view)



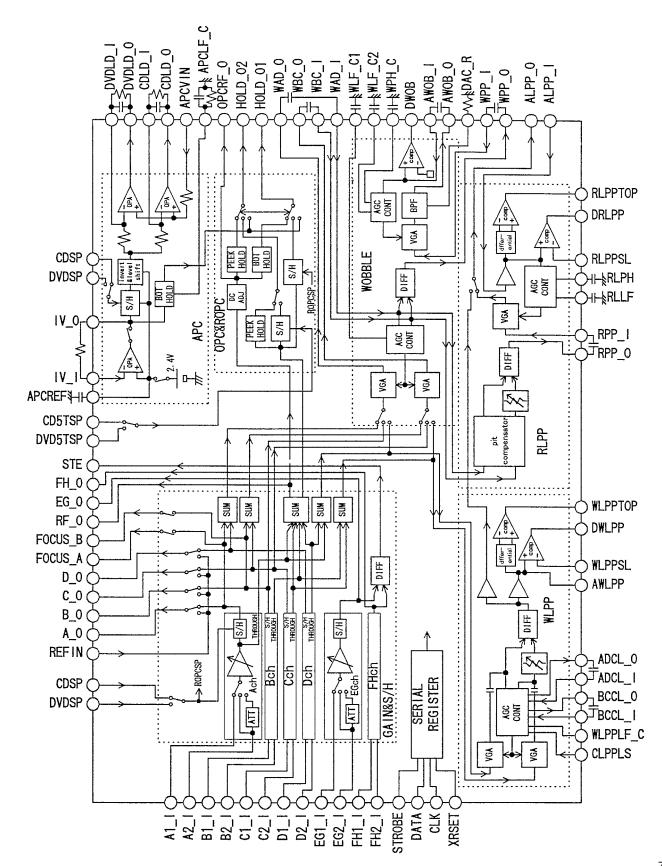
Pin Function

PIN No.	PIN NAME	FUNCTIONS	INTERNAL EQUIVALENT CIRCUIT
1	TC	TPLH Control PIN	
2	SUB	Substrate PIN (*1)	Refer to BLOCK DIAGRAM.
3	GND	GND PIN	
4	Vout	Reset Signal Output PIN	
5	Vcc	Vcc PIN / Voltage Detect PIN	

(*1) Connect to GND.

■ PM0025AF (DVR ATAPI MAIN ASSY : IC109)

- DVD-R/RW Frontend IC
- Pin Arrangement (Top view)



• Pin Function (1/6)

Pin No.	Symbol	I/O	Equivalent circuit	Function
1 2 96 97 98 99	E2G2_I F2H2_I A2_I B2_I C2_I D2_I	I	VCC4 1.5k Sk W Sk W Sk W Sk Sk Sk Sk	A - D, EG, FH signal input (for CD)
90 91 92 93 94 95	A1_I B1_I C1_I D1_I E1G1_I F1H1_I	I	VCC4 OVREF	A - D, EG, FH signal input (for DVD)
3 4 5 6	FH_O EG_O FOCUS_B FOCUS_A	0	VCC4	FH, EG, FOCUS_A - B signal output
5 6	FOCUS_B FOCUS_A	0	200 A 200 A 100k A 110k	FOCUS_A - B signal output
7	RF_O	0	VCC4 50 100k 77 77 77 77 77 77 77 77 77	RF signal output
8 9 10 11	D_O C_O B_O A_O	0	VCC4	A - D signal output
12	REFIN	I	200 200 1	Reference power supply input

• Pin Function (2/6)

	,	·		
Pin No.	Symbol	I/O	Equivalent circuit	Function
13 15 16	DVDSP DVD5TSP DVDAPCSP	I	100K	The sample hold pulse input for DVD (L:hold) DVDSP:S/H Block DVD5TSP:ROPC Block DVDAPCSP:APC Block It is internal 100k and is a pull-up.
17 18 19	CDSP CD5TSP CDAPCSP	I	DVDD1	The sample hold pulse input for CD (L:hold) CDSP:S/H Block CD5TSP:ROPC Block CDAPCSP:APC Block It is internal 100k and is a pull-up.
14	CLPPLS	I	DVDD1 ▲	WLPP clamp pulse input
			100K 3K 3K	It is internal 100k and is a pull-up.
20	DVDD1	-		5V Power supply DGND1 and pair
21	DGND1	-		GND
22 23 24	STROBE DATA CLK	I	OVDD1	3 line serial data input
25 26 27 28 29	MONI TESTA TESTB TESTC TESTD	O I/O I/O I/O		Internal signal monitor terminal
30	XRESET	I	DVDD1	Register reset input (Low:reset) It is internal 25k and is a pull-up.
31	DVDD2	-		5V Power supply DGND2 and pair
32	DGND2			GND
33 34 35 36 37	DWLPP WLPPTOP DRLPP RLPPTOP DWOB	0	DVDD2 DVDD2 So	DWLPP: WLPP 2value-ized output WLPPTOP: RLPP differentiation 2value-ized output DRLPP: RLPP 2 value-ized output RLPPTOP: LPP differentiation in reproduction 2value-ized output DWOB: WOBBLE 2value-ized output It is internal 100k and is a pull-up.
38	VCCA1	_		5V Power supply GNDA1 and pair
39	VREF1	-		Standard voltage 2.1V input GNDA1 and pair
40	GNDA1	-		GND

• Pin Function (3/6)

Pin No.	Symbol	I/O	Equivalent circuit	Function
41 42	RLPPSL WLPPSL	I	VCCA1	LPP slice level input RLPPSL:RLPP Block WLPPSL:WLPP Block
43	TESTSET	I		Test setting terminal
44	AWLPP	0	VOCA1	WLPP Analog output
45	WLPPLF_C		VCCA1	The capacitor connection terminal for WLPP AGC filters
46 48	BCCL_I ADCL_I	I	VCOA1 1.5k 7/7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	WLPP clamp Amplifier input BCCL_I: (B+C)signal side ADCL_I: (A+D)signal side
47 49	BCCL_O ADCL_O	0	VCCA1 Sop The second	WLPP clamp Amplifier output BCCL_O: (B+C)signal side ADCL_O: (A+D)signal side
50	ALPP_I	I	VCCA1	RLPP analog input
51	ALPP_O	0	VCCA1	RLPP analog output

• Pin Function (4/6)

Pin No.	Symbol	I/O	Equivalent circuit	Function
52	RLPH_C	O	4k	The capacity connection terminal for RLPP peak detection
53	RLLF_C	0	VCCAI	The capacity connection terminal for RLPP AGC
54	RPP_I	I	VOCAI	RLPP push pull input
55	RPP_O	0	VCCA1	RLPP push pull output
56	AWOB_O	0	VCCA2	WOBBLE analog output
57	AWOB_I	I	VCCA2 4k 4k 4k 4k 4k 4k 4k 4k 4k 4k 4k 4k 4k	WOBBLE analog input
58	DAC_R	0	VCCA2 WCCA2	The standard resistor connection terminal for DAC
59	VCCA2	-		5V Power supply GNDA2 and pair
60	VREF2	-		Standard voltage 2.1V input GNDA2 and pair
61	GNDA2	<u> - </u>		GND

• Pin Function (5/6)

Pin No.	Symbol	I/O	Equivalent circuit	Function
62	STE	0	VCCA2	STE Output (FH-EG)
63	WPH_C	0	VOCA2	The capacity connection terminal for WOBBLE peak detection
64	WPP_I	I	VCCA2	WOBBLE push pull input
65	WPP_O	0	VCCA2	WOBBLE push pull output
66 67	WLF_C2 WLF_C1	0	VCCAI 100k 100k 100k 100k	WLF_C2: Capacitor connection terminal for WOBBLE AGC WLF_C1: Capacitor connection terminal for WOBBLE RFAGC
68 70	WBC_I WAD_I	I	VCCA2 3k ŠŠ W VPREF	WBBLE B+C (A+D) input
69 71	WBC_O WAD_O	0	VCCA2	WBBLE B+C (A+D) output
72	VCCA3	-		5V Power supply GNDA2 and pair
73	VREF3	-		Standard voltage 2.1V input GNDA2 and pair
74	GNDA3	-		GND

• Pin Function (6/6)

Pin No.	Symbol	I/O	Equivalent circuit	Function
75 76	HOLD_O1 HOLD_O2	0	VCCA2	APC, OPC, and ROPC output terminal
77	OPCRF_O	О	VCCA2	RF signal output (A+B+C+D) for OPEC
78	APCREF	I/O		APC Reference power supply (2.4V) Requires a bypass capacitor to GNDA3
80 82 83 84 85	APCVIN CDLD_I CDLD_O DVDLD_I DVDLD_O	I O I O	VCCA3 VC	APCVIN: APC power setting input CDLD_I: CD APC amplifier input CDLD_O: CD Read power output DVDLD_I: DVD APC amplifier input DVDLD_O: DVD Read power output
81	APCLF_C	О	VCCA2	The capacitor connection terminal for RAPC bottom hold
86 87	IV_0 IV_I	O	VCCA3 VCCA3 VCCA3 SO SO APCREF	IV_O: I/V amplifier output IV_I: I/V amplifier input
88	VREF4	-		Standard voltage 2.1V input GNDA4 and pair
89	GNDA4	-		GND
100	VCCA4	-		5V Power supplay GNDA4 and pair

■ M37902FGCHP (DVR ATAPI MAIN ASSY : IC306)

• CPU

● PinFunction (1/3)

No.	Mark	Pin Name	Туре	Function
1	AN0	OPT_T	I	A / D input of OPC top level
2	TB2IN	BCADATA	ı	BCA DATA input after a party rate
3	TB1IN	TVRCK	ı	TE input for a tracking error count
4	TB0IN	FG	ı	Spindle FG pulse signal input
5	INT2	INT	I	Interruption (for SCSI)
6	INT1	INT	I	Interruption (CD)
7	INT0	INT	I	Interruption (R3,M63)
8	P61	EEPBUS	I	Time BUSY of EEPROM access
9	P60	DISCRW	0	Time High of RW
10	P57	XAUDMUTE	0	AUDIO MUTE (being L MUTE)
11	P56	XCLDON	0	CD LD ON (LOW ACTIVE)
12	P55	XDLDON	0	DVD LD ON (LOW ACTIVE)
13	P54	SPGAIN	I/O	Spindle gain It is usually an input HIZ.
14	P53	BCHIPCS	0	CS of B-CHIP
15	P52	PICGAIN	0	GAIN change in Pickup
16	P51	LDDENBL	0	LD DRIVER ENABLE (being H ENABLE)
17	TA0OUT	LOADPWN	0	PWM output for loading mechanism
18	CS3	CS3	0	CS of S-RAM (negative logic)
19	CS2	CS2	0	CS for address decoders (negative logic)
20	CS1	CS1	0	CS for ENCODER (negative logic)
21	CS0	CS0	0	CS of a flash ROM (negative logic)
22	P43	DVDXCD	0	A change of OPC A / D input (it is CD and H in L and is DVD)
23	P42	ADSEL2	0	A / D multiplexer input change 2
24	P41	ADSEL1	0	A / D multiplexer input change 1
25	P40	ADSEL0	0	A / D multiplexer input change 0
26	P33	XLODMTE	0	Loading drive mute (being L MUTE)
27	XBLW	WR	0	Write strobe (being L write)
28	XRD	RD	0	Lead strobe (it leads by L)
29	XRDY	READY	I	Ready (being H: READY)
30	BYTE	BYTE	I	Bus width setup (8 bits)
31	VCONT	VCONT	0	Filter circuit connection
32	RESET	RESET	I	Power-on reset (it resets by L)
33	MD0	MD0	-	CPU operation mode setup 0
34	VSS	VSS	-	GND
35	XIN	XIN	I	27MHz
36	XOUT	-	-	XOUT
37	VCC	VCC	-	+5V
38	P27	MIRRS1	0	MIRROR signal change setup 1
39	P26	MIRRS0	0	MIRROR signal change setup 0
40	P25	SCS5	0	The serial access strobe signal for I/O EXP

● PinFunction (2/3)

No.	Mark	Pin Name	Туре	Function
41	P24	SCS5	0	The serial access strobe signal for external DAC
42	P23	SCS3	0	The serial access strobe signal for AUDIO DAC
43	P22	SCS2	0	The serial access strobe signal for EEPROM
44	P21	SCS1	0	The serial access strobe signal for A2
45	P20	SCS0	0	The serial access strobe signal for RF63
46	D7	D7	I/O	Data bus 7
47	D6	D6	I/O	Data bus 6
48	D5	D5	I/O	Data bus 5
49	D4	D4	I/O	Data bus 4
50	D3	D3	I/O	Data bus 3
51	D2	D2	I/O	Data bus 2
52	D1	D1	I/O	Data bus 1
53	D0	D0	I/O	Data bus 0
54	MD1	MD1	I	CPU operation mode setup 1
55	VSS	VSS	I	GND
56	P07	XRST	0	SYSTEM RESET (resets: L)
57	P06	DET3T	I	3T DETECT signal input
58	P05	TZCHYS0	0	Tracking zero crossing hysteresis change 0
59	P04	TZCHYS1	0	Tracking zero crossing hysteresis change 1
60	A19	A19	0	Address bus 19
61	A18	A18	0	Address bus 18
62	A17	A17	0	Address bus 17
63	A16	A16	0	Address bus 16
64	A15	A15	0	Address bus 15
65	A14	A14	0	Address bus 14
66	A13	A13	0	Address bus 13
67	A12	A12	0	Address bus 12
68	A11	A11	0	Address bus 11
69	A10	A10	0	Address bus 10
70	A9	A9	0	Address bus 9
71	A8	A8	0	Address bus 8
72	A7	A7	0	Address bus 7
73	A6	A6	0	Address bus 6
74	A5	A5	0	Address bus 5
75	A4	A4	0	Address bus 4
76	A3	A3	0	Address bus 3
77	A2	A2	0	Address bus 2
78	A1	A1	0	Address bus 1
79	A0	A0	0	Address bus 0
80	TXD1	TXD1	0	RS232C transmission

DVR-A03

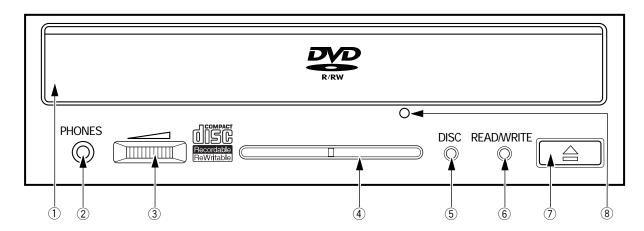
● PinFunction (3/3)

No.	Mark	Pin Name	Туре	Function
81	RXD1	RXD1	I	RS232C reception
82	P85	XDMUTE	0	BTL driver mute
83	P84	BCHIPINT	I	Interruption of B-CHIN
84	TXD0	SD0	0	Synchronous serial transmission
85	RXD0	SDI	I	Synchronous serial reception
86	CLKD0	SCLK	0	Synchronous serial clock
87	VCC1	VCC	-	+5V
88	AVCC	AVCC	I	Analog power supply (+5V)
89	VREF	VREF	I	Standard voltage input (+3.3V)
90	AVSS	AVSS	I	GND
91	VSS	VSS	I	GND
92	NMI	NMI	I	-
93	DA1	EPWDA2	0	DAC output for an erase power
94	P77	FGIN	0	FOCUS gain change signal
95	DA0	RPWDA	0	Read power offset adjustment value output
96	P75	LDIDET	I	LD DRIVER current value detection
97	AN4	MPXAD	I	ADC Input (signal after MPX)
98	AN3	LEM	I	A/D Input for Lens error
99	AN2	TLER	I	A/D Input for Tilt error
100	AN1	OPEC_B	I	A/D Input of OPC bottom level

8. PANEL FACILITIES AND SPECFICATIONS

8.1 PANEL FACILITIES

Front Panel



1 Disc Loading Tray

Open the loading tray by pressing the eject button, then place a CD or DVD disc into the slit with the label facing up. Press the eject button or push the front part of tray to load the tray with the disc.

② Headphone Jack (PHONES)

Stereo mini jack for head-phone.

Set "Volume Control Knob" minimum position before inserting headphone jack.

The audio output of rear panel is active even when a jack is inserted into the headphone plug.

③ Volume Control Knob

This is the volume control knob for adjusting sound level on the headphone.

When the knob is turned to the right, the headphone volume goes up, when turned to the left, the volume goes down.

4 Ventilation Holes

Do not block this part.

5 DISC Indicator

Lights when a disc has been inserted.

When tray is opened or closed
Read only disc
Recordable disc
Unsupported disc
Lights green
Lights orange
Blinks orange

6 READ/WRITE Indicator

Operation status is indicated as follows.

During reading

During writing

When an error occurs

Lights orange
Blinks orange

When an error occurs Blinks oranAbnormal rise of internal temp

emp

• Blinks 1x and then repeats
• Blinks 2x and then repeats
• Blinks 3x and then repeats

• Other error ⑦ Eject Button (♠)

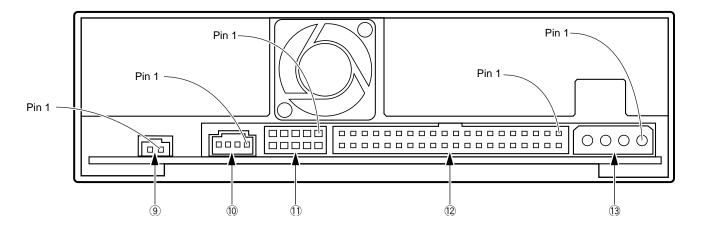
To unload /load the disc, press the button.

8 Forced Ejection Hole

· Lens or disc dirty

Insert a stiff rod into the hole and push to eject the tray when the tray doesn't unload by pressing the Eject button. In the normal operation, the eject button should be used to unload the tray. Make sure the power of the drive is turned off and wait more than one minute till the disc rotation is stopped when access the eject hole.

Rear Panel



9 Digital Audio Output

This is a connector for output of digital audio signal.

Pin	Name	Function
1	GND	Ground.
2	Digital Out	Digital audio signal output.

10 Audio Output

This is a connector for output of analog audio.
This connector is compatible with `Molex 70553`, choose a suitable connection cable.

Pin	Name	Function	
1	L	Left channel audio output.	
2	G	Ground.	
3	G	Ground.	
4	R	Right channel audio output.	

1) Device Configuration Jumper

Switch becomes ON when short socket is put.

Make sure the power of the drive is off before changing jumper setting. Pin # 1 is ON at the time of shipping from the plant.

Pin	Name	Function	
1	MA	on The drive is used in master mode.	
2	SL	on	The drive is used in slave mode.
3	CS	on	Using Cable Select function.
4		Reserved.	
5		Reserved.	

12 Host IDE Interface

This is a 40 pin I/O connector according to the ATA specifications.

13 DC Input

Pin	Name	Function	
1	+12	Power supply input for DC +12 V.	
2	G	Ground.	
3	G	Ground.	
4	+5	Power supply input for DC +5 V.	

8.2 SPECIFICATIONS

[Setting] This drive is Horizontal Use. [Disc Size] • 120 mm (4.72") / 80 mm (3.5") [Data Transfer Rate] Data Read (Sustained) CDMax. 3.600 KBvtes/sec. (10.3 – 24X CAV Mode over 16 block transfer) Data Write (Sustained) CD Ave. 1,200 KBytes/sec. (8X CD-R) Host Interface specification • The data transfer rate may not be output due to disc conditions (scratches, etc.). [Access Time/ Seek Time] Access time (Random average) Seek time (Random average) [Audio Characteristic] [Others] Power Supply (including front panel)5-27/32 (W) x 1-11/16 (H) x 8-5/32 (D) in. [Accessories] Short-circuit socket x 2 Audio cable x 1 Mounting screw x 4 Push rod x1

NOTE:

Operating instructions x 1

• Specifications and design subject to possible modifications without notice, due to improvements.

